Late Breaking Results: Single Flux Quantum based Brownian Circuits for Ultra-Low-Power Computing

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***Abstract*—This paper proposes a random walk circuit implementation with single flux quantum devices, essential for Brownian circuits, to reduce processing energy consumption dramatically. SPICE-based simulation demonstrating its functional operation and random walks can be achieved via the Shapiro-Wilk test. Furthermore, we developed a Monte Carlo simulator for Brownian circuits, enabling functionality verification and computation step distribution analysis. Latency/energy evaluation using a half-adder as a case study revealed that proposed circuits could reduce energy consumption by 1/1260 and offer an opportunity for low-power computing systems.**

I. Introduction

With the advent of the post-Moore era, achieving sustainable low power consumption and improved computer performance has become a challenge. As a significant solution to this problem, much research is focusing on computing with emerging devices. Superconducting devices that can manipulate a single flux quantum (SFQ) as an information carrier are one of the most promising technologies and have attracted attention from academia and industry, with prospects reported in IRDS. Well-designed SFQ computer systems showed high performance and low power consumption [1].

However, since the computational principles are conventional, noise suppression is an essential issue in these methods. Ultimately, it becomes the bottleneck that degrades the efficiency of the computer. In other words, although any information carrier will eventually consist of only a few particles or quanta (e.g., electrons or photons) to compose a signal, the signal strength must be maintained above a certain level against fluctuations. For example, SFQ-based AI accelerators consume most of their energy to operate stably against fluctuations [1]. To overcome the noise limit problem and realize an ultra-low-power computer, it is necessary to break away from the idea of "noise suppression" and explore other computational principles.

Our research proposes implementing Brownian circuits (BC) with SFQ devices to make a breakthrough in the noise limit issue and reduce processing energy drastically. We have focused on the unique features of SFQ devices and found a high affinity for BC. This paper shows the implementation of a random walk circuit with SFQ devices, the most basic and essential one, and the low energy consumption of SFQ-BC. As far as we know, this is the first implementation of random walk for BC with SFQ devices. Our contributions are summarized as follows:

- We proposed an SFQ circuit implementation of a random walk circuit and verified its operation by SPICE-based simulation. The Shapiro-Wilk test proved that the distribution of SFQ locations in the circuit follows a Gaussian distribution and random walkability.
- We developed a Monte Carlo simulator for the BC. The simulator allows us to verify BC's functionality and analyze the distribution of the number of steps required to complete the processing.
- We evaluated the latency and energy for the half-adder as a case study, showing that the proposed SFQ-BC can achieve an energy reduction of 1/1260x compared to conventional.

II. SFQ based Brownian circuits

A. Limitaions of Traditional SFQ Design

SFQ circuits use quantized magnetic flux (SFQ) as the information carrier in a ring of superconductors. As shown in Fig. 1, an SFQ ring consists of two Josephson junctions (JJ), which consist of two superconductors coupled by sandwiching a tunnel barrier layer, such as an insulator (AlO_x) between them. A JJ normally allows the current to flow without a potential difference. However, when a current exceeds the critical current value (I_c) flows, circulating current through the ring moves to the adjacent ring, i.e., propagation of the SFQ, and a voltage across the junction is generated. Conventional SFQ circuits calculate by moving the SFQ in one direction by sophisticated control of the current flowing in the JJs and passing through SFQ-logic gates such as AND, OR, and NOT [1].

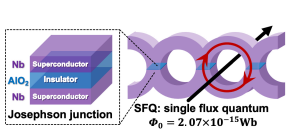

Fig. 1. SFQ devices

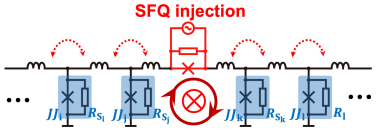

Fig. 2. SFQ Random walk circuit

While conventional SFQ devices can switch extremely fast ($\sim$ 1 ps) and low-energy ($\leq$ 0.1 aJ), further low energy consumption is limited by noise tolerance. In other words, to induce a stable switching without noise disturbance, I_c is designed to be approximately 100 times larger than the noise, and the circuit is driven by controlling the bias voltage source and the clock signal. Unfortunately, the bias power supply consumes over 95% of the entire power, and the clock line occupies a quarter of the circuit in the SFQ-AI accelerator [1]. We should explore other computational principles to achieve dramatic energy reductions beyond the noise limit.

B. SFQ-based random walk for Brownian circuit

BC is one promising approach to making a breakthrough in the noise limit; The idea is to miniaturize a mechanical Turing machine and explore the circuit topology while the signals move around randomly in the machine [2]. The key concept is that fluctuations are not suppressed factors in these circuits but are aggressively used to support the computation. Therefore, it is essential to realize a random walk circuit. Although this method theoretically reduces the energy required for information processing to the limit, it is challenging to implement in an actual circuit. That is because it requires both reducing the signal level so that devices can be driven by noise and ensuring a signal-noise ratio that can measure the signal.

We focus on the unique features of SFQ devices and their high affinity to BC. The intrinsic switching threshold is close to the noise level, and the magnetic flux is quantized and constant ($\Phi_0 \fallingdotseq 2.07 \times 10^{-15}$ Wb) independent of the threshold. It means that SFQ devices can be both driven by noise and measure signals. Noise triggers the SFQ to move in a random walk circuit, so I_c must be the same as the noise intensity level. The dominant noise in SFQ circuits is Johnson noise [3], with an intensity of around 1 μA ($= \sqrt{4k_BT\Delta f/R_s}$). Fig. 2 shows the circuit diagram of the proposed SFQ random walk. When the red voltage source and JJ inject SFQ forcibly, SFQ is held in the loop of JJ_j and JJ_k. After that, SFQ tokens are randomly searched in the circuit by Johnson noise. For example, if JJ_j switches before JJ_k dose, the SFQ transitions to the left side.

In the proposed circuit, each JJ switches asynchronously and independently with unintended timing, which is not computable with conventional logic gates. Reversible gates such as Hub and CJoin, shown in Fig. 3(a)-(b), are required to process with random walk search. The set of reversible gates has been proven to be one of the functionally complete sets [4]. A single SFQ, denoted by a blue blob, randomly walks on a line as a token. Hub gates are intersections connecting three lines; a token can move between the lines in any order. The CJoin gate has one token on each of the two input lines. Both tokens move onto the output line when on the input line. It also works reversibly. If there is only one token on one input line, it will continue to randomly walk on the line until the other token arrives on the other, i.e., it cannot pass through the gate.

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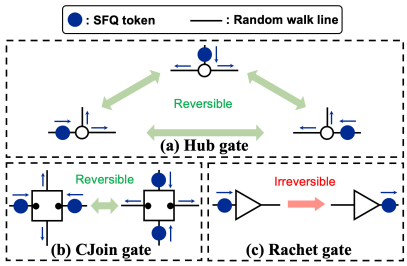

Fig. 3. Universal reversible gate set

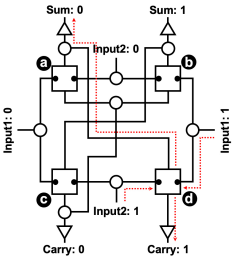

Fig. 4. Half-adder

C. Case for Half-Adder Design

An example of an arithmetic unit using these gates, a half-adder (HA), is shown in Fig. 4. Input and output have unique ports indicating "0" and "1", respectively. When an SFQ token exists at [Input1: 1], this means that the logic value of input1 is "1", and no token should exist at [Input1: 0] simultaneously. For example, when executing "1" + "1", the token input from [Input1: 1] moves randomly along the line between the CJoins at ⓑ and ⓓ, and the token from [Input2: 1] does the same. Only when the two tokens arrive at the ⓓ CJoin do they pass through the gate and arrive at [Carry: 1] and [Sum: 0]. Every output port has a ratchet gate (Fig. 3 (c)), an irreversible gate. The fact that the arithmetic unit consists entirely of reversible gates means that tokens arriving at the output ports can be reversed back to the input ports. To prevent the back-flow, a ratchet gate at the output port acts as a valve to trap the token for computation in the finished state.

D. Monte Carlo simulator for Brownian circuits

Since BC leave token movement to noise, the number of moving steps required for the computation is nondeterministic. Therefore, we have developed a Monte Carlo simulator for SFQ-BC with Python. Supported gate sets are Hub, CJoin, and Ratchet gates. By inputting arbitrary circuit information as a netlist, the simulator can visualize the calculation process and provide the probabilistic distribution of the steps to finish the calculation. The tool supports verifying that an arbitrary circuit meets the functional specifications and estimating the latency and energy consumption depending on the number of steps.

III. Experimental Results

A. Verification of the SFQ random walk circuit

We verify that the proposed circuit satisfies the functional specification, i.e., the SFQ moves randomly with Johnson noise. We designed the proposed superconducting circuit using JoSIM, a SPICE-based circuit simulator [5]. A noise current source simulating the Johnson noise generated at the shunt resistor (R_s) in Fig. 2 is inserted in parallel with JJs. This experiment assumes $I_c = 2.15\ \mu$A, an operating environment of 4.2 kelvin, and $R_s = 184\ \Omega$.

We assume the random walk moves by $\pm\sigma$ with probability $1/2$ per step. It is well known that the token's position $r(t)$ after t steps follows a Gaussian distribution ($r(t) \sim N(0, \sigma^2 t)$) [6]. Therefore, we apply the Shapiro-Wilk test to the SFQ positions obtained by JoSIM.

Firstly, Fig. 5 shows the trajectories of the SFQ positions for 100 JoSIM simulations. The vertical axis shows the SFQ position, with 0 as the starting point, and the SFQ diffuses as the step progresses. An interesting point is that the possibility of searching a wider area increases as the step progresses. This is consistent with the fact that theoretically, the variance of the distribution after the t steps is $\sigma^2 t$.

Secondly, Fig. 6 shows the histogram of SFQ locations at 100 steps superimposed on an ideal Gaussian distribution. Applying the Shapiro-Wilk test, the p-value is 0.384. Since the significance probability ($p = 0.384$) is greater than 0.05, the location of the SFQ is proven to follow a Gaussian distribution. As the result, the proposed circuit has a random walk operation.

B. Latency and energy evaluation

We evaluate the latency and energy of SFQ-BC using the half-adder as a case study. The latency of an SFQ-BC can be estimated as $[switching\ latency] \times [\#\ computation\ steps]$. The switching latency of JJ is assumed to be 1.4 ps [7]. Fortunately, the proposed circuit has no static energy due to no bias voltage source and only dynamic energy. Therefore, the energy can be calculated as $[switching\ energy] \times [\#\ computation\ steps]$. The following equation can calculate one switching energy: $I_c \Phi_0 \fallingdotseq 4.45 \times 10^{-21}$ J.

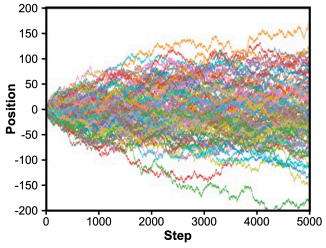

Fig. 5. SFQ's moving trajectory

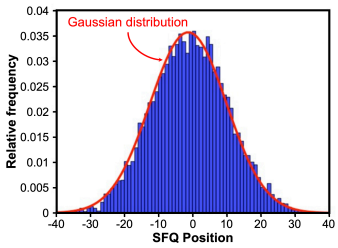

Fig. 6. Histogram of SFQ positions

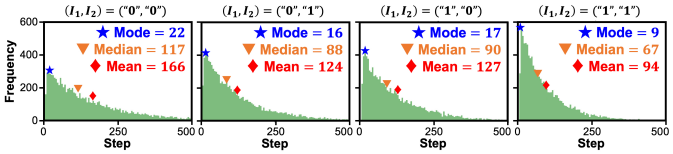

Fig. 7. Histograms of the number of steps required to execute half-adder

TABLE I
Latency and Energy Comparison

	Latency [ps]	Energy [aJ]	EDP [qJs]
CMOS-HA (180nm) [8]	310	43×10^3	13×10^6
Conv. SFQ-HA (1μm) [9]	**37.8**	718	27×10^3
Prop. BC-based SFQ-HA (1μm)	179	**0.57**	**102**

The number of calculation steps, an essential factor in latency and energy evaluation, was analyzed using our Monte Carlo simulator, and the results are shown in Fig. 7. The histogram of the number of steps required to reach the end state of the calculation for each input pattern (I_1, I_2) provides the mode, median, and mean values, respectively. The mode is located in small steps as a peak, where the probability decreases exponentially. The histograms vary with the input pattern, and this difference depends on the length of the random walk line. Fig. 4 shows that the path length from each input set to its own goal is not uniform. This paper assumes that the average of all input sets ($= 127.6$) is the required steps to for the half-adder calculation.

Finally, we summarize the results of latency and energy comparisons based on this analysis in Table I. The proposed BC-based half-adder compared to one designed using the PDK 180 nm bulk CMOS process node [8] and a conventional SFQ circuit with AIST 1.0 μm process [9]. Note that these exclude the cost of cooling the SFQ circuits. The table shows that our proposed circuit can perform operations with extremely low energy (1/1260x) compared to the conventional SFQ-HA. On the other hand, the latency is increased by a factor of 4.7x due to the steps required for the random walk search. However, thanks to the potential high speed of SFQ devices, the latency is shorter than that of CMOS. In conclusion, the SFQ-based BC indicated sufficient potential to realize ultra-low power circuits.

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