A Scalable Low-Latency FPGA Architecture for Spin Qubit Control through Direct Digital Synthesis

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***Abstract*—Scaling qubit control is a key issue for Large Scale Quantum (LSQ) computing and hardware control systems are increasingly costly in logic and memory resources. We present a newly developed compact Direct Digital Synthesis (DDS) architecture for signal generation for spin qubits that is scalable in terms of waveform accuracy and the number of synchronized channels. Fine control of gate voltages is achieved by on-the-fly generation of very precise ramps. Embedded memory requirements are reduced by orders of magnitude compared to current Arbitrary Waveform Generator (AWG) architectures, removing a major scalability barrier for quantum computing.**

***Index Terms*—direct digital synthesis (DDS), FPGA, large scale quantum computing (LSQ), quantum control, spin qubits**

I. Introduction

Quantum computers need error correction to achieve quantum advantage. They also require calibration of large sets of parameters for the correct operation of qubits, which can take several hours for Google Sycamore with only 53 qubits. Scaling up quantum computing requires fast, scalable and flexible feedback to implement Quantum Error Correction (QEC) and accelerate calibration. Both QEC and calibration require electronics with the ability to measure, compute and apply feedback with the lowest possible latency. This must scale to thousands of qubits using today's electronics. FPGAs are the ideal choice as they can be reprogrammed to meet varying experimental needs while achieving very low feedback latency.

A typical qubit manipulation experiment (Fig. 1) involves a network of FPGAs at room temperature handling the qubit feedback loop through Digital to Analog Converters (DACs) and Analog to Digital Converters (ADCs). For spin qubits, control signals consist of two types. First, quasi-static controls that are based on nanosecond ramps to tune the potential well and coupling of qubits in order to change their states. Secondly, radio frequency pulses, controlled through I/Q modulation, which are used for measurements or resonance-based control. Digital mixing is used to achieve more complex control schemes and pulse engineering. Full digital generation increases flexibility and reduces noise sources.

We present a scalable, complex signal generator (CSG) using on-the-fly generation of ramps and frequency combs to reduce the memory requirements and to enable sub-nanosecond scale dynamic signal synthesis. Our primary contribution is a novel ramp generator which generates all the points required at the oversampled DAC frequency using a fraction of the memory compared to State of the Art (SoA) solutions.

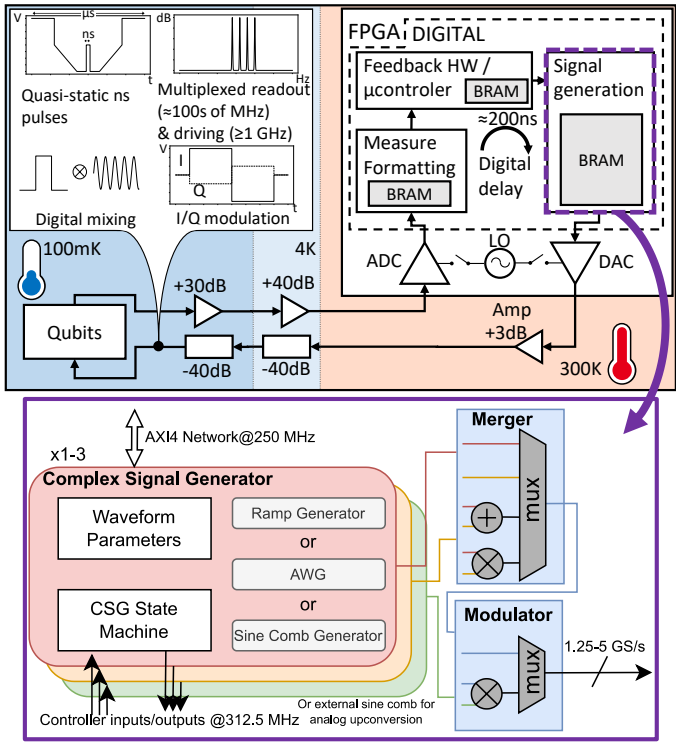

Fig. 1. Qubit Manipulation: Proposed Architecture for Spin Qubit Control

The design can mix several sources between a ramp generator, a sine wave generator and an AWG to create complex signals. The sine generator can create up to 16 frequencies and the ramp generator achieves temporal controllability at the higher DAC sampling frequency up to 5 GS/s which is critical for high fidelity qubit control. We use digital up-conversion of frequency combs up to 5 GHz, to avoid the noise from analog mixers. The design has been validated in hardware on a ZCU111 FPGA board from Xilinx.

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II. Architecture for Direct Digital Synthesis

The design can multiplex I/Q modulation or feed quasi-static signals to each DAC (Fig. 2). Each CSG has its own controller, as a distributed design enables better scalability. CSGs are highly configurable and can mix up to three generators: AWG, sine comb generation and ramp generation (Fig. 1). An AXI network allows data transfer between our software layer and the CSGs. The embedded software compiles waveform parameters, selects bitstreams and performs initialization providing the bridge between the physics of qubits and quantum computing.

Existing algorithms to generate ramps on-the-fly [1] can not achieve high oversampling, as they are limited to interpolation. Our ramp generator pipeline computes an intermediate representation with ramp coefficients on one side and control metadata on the other to generate ramps on-the-fly. This approach enables controlability at the sampling rate of the DACs to generate up to 16 ramps per clock cycles. The sine wave generator creates up to 16 sines in a comb for multiplexing.

This innovative architecture only requires a 312.5 MHz working frequency to control 5 GS/s signals. A single, standard DAC channel uses less than 2% of the FPGA logic resources, leaving a large part of the FPGA fabric to implement hardware feedback such as QEC. The entire design is highly configurable, especially regarding memory requirements and dynamic reconfiguration enables quick switching between experiments.

A feedback sequence (ie. from parameter change to DAC entry) for a ramp generator takes 76.8 ns. The sine generator takes at most 48 ns for full feedback. Competing AWG-based systems take several microseconds for comparable signal updates since the full waveform needs to be re-written. Of course, this design can still quickly switch between existing waveforms like AWGs systems. Quick feedback is essential for QEC and reduces the time required for calibration.

III. Measurements and Scalability

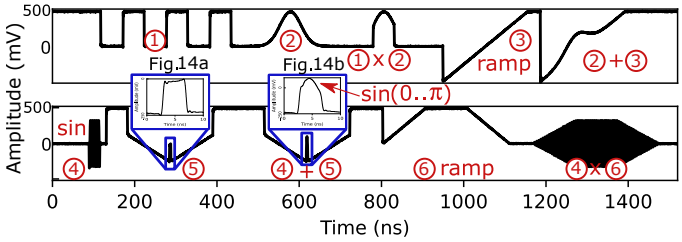

Fig. 2. Measurements of two DAC channels (oversampling factor of 16, 5 GS/s)

After calibration, sine wave generation is clean over a wide band before upconversion. Indeed, the Spurious Free Dynamic Range (SFDR) is above 60 dBc up to 350 MHz, which is far above the typical SFDR of upconversion frequencies [2]. Phase noise (PN) slightly increases with the frequency generated but stays under -100 dBc/Hz for in-band PN up to 450 MHz. When multiplexing 16 frequencies, SFDR of the higher frequency sine (320 MHz) is reduced to 48 dBc but the PN does not increase.

In SoA AWG architectures, the memory resources scale linearly with the DAC sampling rate, whereas in our DDS architecture, the memory resources depend only on the complexity of the waveform. Thus, the bandwidth and capacity

	on-the-fly generation		digital mixing	Fast HW feedback	Qubit focus
	ramps	sine wave			
COMPAQT[4]	X	X	X	X	superconducting
Yang & al.[5]	X	X	X	switch only	superconducting
QUBIC[6]	X	X	X	switch only	superconducting
ICARUS-Q[7]	X	X	X	switch only	superconducting
QICK[8]	X	single-tone	sine only	✓	superconducting
Presto[9]	X	multi-tone*	sine only	✓	superconducting
This work	16/cycle	multi-tone	✓	✓	spin qubits

Fig. 3. State of the Art of Control Architectures for Qubit Manipulation. **Achieved by using multiple DACs per channel.*

issues associated with AWG-based architectures are alleviated. For instance, applying a SWAP gate (⑤ in Fig. 2) to 24 pairs of spin qubits [3] would require 248 waveform parameters and instructions (1.2 KB) with our architecture while AWG-based architectures would need 210 KB of data. Using the DCT and RLE compression schemes from COMPAQT [4], at the same accuracy, this figure drops to 55.9 KB which still represents 46.5× more data to transfer and store than our work.

When using RF control of spin qubits, digital multiplexing reduces the number of AC cables by up to 16×. Adding analog multiplexing even allows our architecture to drive up to 32 qubits through one AC-cable using a single board, with space for six additional quasi-static controls.

IV. Conclusions

SoA Architectures (Fig. 3) [4]–[9] do not simultaneously provide quality ramp generation, fast hardware feedback capabilities, flexibility and digital-only multiplexing. Our architecture achieves SoA qubit control, tailored for spin qubits by providing hardware for on-the-fly signal generation, replacing the very large memories storing pre-calculated data for AWGs. We demonstrate a 175× memory reduction compared to approaches based on AWGs. The low memory requirements and low feedback latency of our device directly translate to a significant reduction in calibration time, up to two orders of magnitude on some steps, which is a major overhead in quantum computers. Signal multiplexing reduces the number of cables into the cryogenic refrigerator. Combined, these contributions represent a significant advance in spin qubit control.

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