Challenges and Unexplored Frontiers in Electronic Design Automation for Superconducting Digital Logic

Sasan Razmkhah
Ming Hsieh Department of ECE
University of Southern California
Los Angeles, CA, USA
razmkhah@usc.edu

Robert S. Aviles
Ming Hsieh Department of ECE
University of Southern California
Los Angeles, CA, USA
rsaviles@usc.edu

Mingye Li
Ming Hsieh Department of ECE
University of Southern California
Los Angeles, CA, USA
mingyel@usc.edu

Sandeep Gupta
Ming Hsieh Department of ECE
University of Southern California
Los Angeles, CA, USA
sandeep@usc.edu

Peter A. Beerel
Ming Hsieh Department of ECE
University of Southern California
Los Angeles, CA, USA
pabeerel@usc.edu

Massoud Pedram
Ming Hsieh Department of ECE
University of Southern California
Los Angeles, CA, USA
pedram@usc.edu

***Abstract*—Positioned as a highly promising post-CMOS computing technology, superconductor electronics (SCE) offer the potential for unparalleled performance and energy efficiency gains compared to end-of-roadmap CMOS circuits. However, achieving very large-scale integration poses numerous challenges. These challenges span from the modeling and analysis of superconducting devices and logic gates to the intricate design of complex SCE circuits and systems. Addressing power and clock distribution issues, minimizing adverse effects of flux trappings, and mitigating stray electromagnetic fields in sensitive SCE circuitry are key challenges that need attention. Verification and testing of SCE circuits also remain open problems. Moreover, scaling the minimum feature sizes of SCE circuits, currently set at 150nm, presents critical scaling and physical design challenges that must be overcome. This review aims to delve into these issues, providing detailed insights while exploring existing or potential solutions to overcome them.**

***Index Terms*—Superconductor Electronics, Single Flux Quantum Logic, Digital Logic, Electronic Design Automation**

I. Introduction

Since the groundbreaking discovery of superconductivity by Onnes in 1911, there has been a surge of enthusiasm for exploring new physics and harnessing its potential for innovative devices. Superconductors derive their name from their zero resistivity when reaching a critical temperature. However, their distinct characteristics, including perfect diamagnetism and thermodynamic transitions, set them apart from perfect conductors. These unique properties have paved the way for the development of cutting-edge devices such as quantum-sensitive sensors like photon detectors and SQUID magnetometers, subterahertz electronics including ADCs, and high-speed digital circuits like rapid single flux quantum (RSFQ) and adiabatic quantum flux parametron (AQFP), as well as the more recent field of quantum computing [1].

The main component in superconductor circuits is the Josephson junction (JJ). JJs are created by a weak link, such as sandwiching a non-superconductor layer between two superconductors, and they operate based on the principles of quantum tunneling. The behavior of JJs is estimated by a set of equations known as Josephson AC and DC equations. As nonlinear elements, JJs can switch and generate rapid picosecond pulses, each carrying the precise energy of one flux quantum (Φ_0), known as SFQ. These pulses are integral in digital superconductor circuits for processing and propagating information [2].

Superconductors, while offering numerous advantages, face challenges in large-scale electronics implementation. The need for extremely low temperatures for cooling restricts their use in standard industry or laboratory setups. Fabrication processes for superconductor materials lag behind CMOS counterparts, and the intricate physics and the unavailability of precise models make developing resilient superconductor electronics challenging [3]. Operating on quantum mechanics principles requires Electronic Design Automation (EDA) tailored to the properties of these devices and must accommodate diverse SCE operating conditions.

Due to superconductors' nonlinearity and quantum characteristics, developed EDA tools rely on approximate models and numerical solutions for solving even basic devices. Van Dozer et al. introduced the SPICE-inspired circuit solver, Josephson Simulator (JSIM), at Berkeley [4]. JSIM utilized the resistively and capacitively shunted junction (RCSJ) model for JJ-based circuits, valid at $T << T_C$, and can add white noise and transmission line models. Programs such as WR-SPICE [5] in the XIC tool suite further contributed to advancing SCE

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by introducing GUI. To model temperature effects in SCE, including quasiparticle current, a Portable Superconductor Circuit Analyzer (PSCAN) was developed by Polonsky et al. [6]. The L–meter was used to extract inductances and calculate the layout area [7]. Still, it fell short in extracting mutual couplings, considering the effects of current and temperature, kinetic inductances, and parasitic capacitances in superconductor layers. At the time, no tools were available for architecture-level design, circuit synthesis, placement and routing, verification, and fabrication process simulation.

The ColdFlux/Supertools project [8], led by the University of Southern California, marked a significant breakthrough in addressing the deficiency of design, simulation, and verification tools for SCE. The qPALACE tool suite emerged as a comprehensive set of tools, covering high-level architecture translation, cell-level design, placement and routing, signal and clock path optimization, and GDSII layout creation. The project also introduced the analog simulator JoSIM, incorporating numerous advanced features. Within this initiative, TCAD code FLOOSS was developed to simulate the fabrication process and extract JJ parameters. At the same time, Inductex expanded its capabilities for extracting inductance and other parasitic parameters from the layout, including capacitances and simulating flux trapping in circuits.

While the ColdFlux tool suite (available at coldflux.usc.edu) represents a significant advancement in EDA, a substantial gap persists. Existing technologies like RSFQ and its derivatives (e.g., ESFQ) mimic the structure of CMOS for computing. While these technologies exhibit superior speed and power efficiency compared to traditional CMOS circuits, the lack of logic density and reliable dense memory presents substantial obstacles to further developing SFQ and SFQ-based technologies. To fully harness the potential of SCEs, there is a critical need for innovative architectures, logic gates, and a paradigm shift in data storage and propagation.

Recent publications, including reciprocal quantum logic (RQL) [9], Pulse Conserve Logic (PCL) [10], phase logics [11], and stochastic computing cores [12], offer promising directions for SCEs. Additionally, the pulsed nature of SCEs, coupled with similarities to the biological brain, positions them as ideal candidates for exploring spiking neural networks (SNN) [13]. Therefore, numerous opportunities exist for developing novel devices and architectures within superconductor electronics. All these technologies and architectures need specialized EDA tools to synthesize, simulate, and verify the circuits.

This survey delves into the challenges faced in superconductor digital logic and examines how these challenges have been addressed and overcome or if they still require attention. As architectures become more intricate and the exploration of novel devices and applications continues, new challenges will likely emerge. We categorize these challenges into three key areas: circuit and architecture, verification and testing, and integration with conventional technologies. We also discuss some new frontiers and the potential of superconductor logic.

II. Superconductor Digital Logic

Most SCEs focus on generating and propagating magnetic flux, particularly SFQ. In contrast to CMOS, SFQ-based logic employs a fast pulse to represent the existence of data. These pulses, lasting only a few picoseconds and with an amplitude $\approx$1 mV, result in power consumption that is 1000$\times$ lower than CMOS. However, this logic requires synchronization, with the clock pulse distinguishing between the zero state and no data. Consequently, each logic gate in these circuits requires a clock signal for data generation and propagation. The validity of the data is confined to the timeframe of the clock pulse, emphasizing the critical nature of balancing data and clock signal paths. Due to data quantization, branching is impractical, leading to very limited fan-in and fanout and the requirement for specialized circuits known as splitters to increase fanout.

QFP-based technology does not depend on junction switching to generate pulses. Consequently, it is significantly more power-efficient, utilizing current levels to determine zero or one values. However, data propagation is facilitated by the AC bias current, acting as a clock signal while supplying energy for circuits. AQFP circuits exhibit a power consumption that is 100 times lower than SFQ. These circuits are adiabatic, so the logic frequency cannot exceed approximately 5 GHz. Since AQFP is reversible and current propagates in superconductors without resistance, the only power consumption is attributed to fabrication imperfections and radiation. However, the need for inductive coupling and transformers made these circuits bulkier than other SCEs. Figure. 1 demonstrates the two leading SCE technologies.

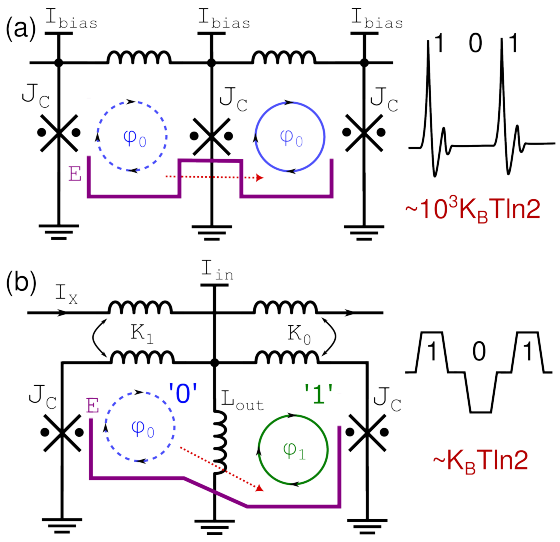

Fig. 1. Two main technologies in use for SCEs. (a) RSFQ works based on generating and propagating the SFQ pulses by switching JJs. (b) AQFP works on the principles of adiabatic transition of the flux and change in the state. Hence, no switching occurs, and while slower than RSFQ, it is more power efficient.

These represent the two primary families of SCE. Other, less-known, and newer families either operate based on one of the mentioned mechanisms or a combination thereof, except for QPSJs, where the geometry induces a change in the phase of the superconducting wave function, temporarily disrupting

superconductivity and creating a voltage. Consequently, this device's current and voltage relations are opposite to the JJs, whose logic is voltage-based.

III. Challenges in SCE Design, Implementation, and Operation

Developing a new technology like SCE presents a myriad of challenges and opportunities. The ongoing challenges hindering the development of SCE are demonstrated in Fig. 2. These challenges revolve around the scalability of logic operations and the insufficient density in memory design. While enhancements to the fabrication process can tackle aspects such as device dimensions, the number of interconnect layers, and parameter margins, certain issues require attention at the circuit and architecture levels. Specifically, the lack of scalability is attributed to the high bias currents essential for cryogenic circuit operation, limited fan-in/fanout, a deep pipeline structure with a large clock tree, and a compact memory design. Moreover, the interface between SCE and conventional circuits can be challenging due to the need for high amplification and data busses that operate across large temperature gradients.

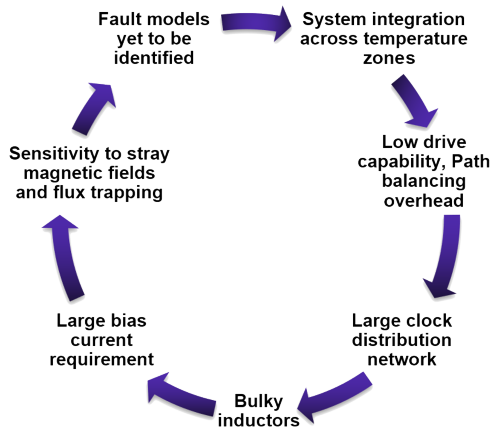

Fig. 2. The main challenges in SCE logic design, implementation, and operation. New fabrication, circuit design, architectural techniques, EDA tools, or a combination can address these challenges.

A dependable fabrication process with favorable parameter margins necessitates exploring innovative techniques and materials, often entailing significant costs. The task of creating new devices with desirable characteristics that are also reproducible poses a notable challenge. The current state-of-the-art fabrication for superconductor chips involves 200mm wafers with a 120nm feature and nine superconductor layers, as exemplified at MIT Lincoln Laboratories [14]. This configuration provides two interconnect layers. However, compared to the 300mm, 2nm node CMOS process with 15 interconnect layers, the superconductor process appears relatively primitive.

Consequently, most of the area budget is allocated to the expansive cell area, the signal and clock distribution tree, and the bias distribution network. Furthermore, niobium, a key material in this process, has a rough surface, which makes planarization and increasing layer number costly and is susceptible to oxidation, forcing lower temperatures in fabrication that yield a lower barrier quality. Therefore, innovations in methods, new superconductors, and barrier materials are imperative for enhancing the fabrication process.

The emerging paradigms in novel architectures necessitate specialized design and verification in EDA. For innovative magnetic devices like 2ϕ-JJ, π-JJ, and logics like the all-JJ family, including half flux quantum (HFQ) [15] and phase logic circuits [11], there exists a shortage of suitable models, simulation tools, and tailored architecture. Similarly, novel nanowires-based devices like the quantum phase slip junction (QPSJ) lack appropriate models and design tools. Therefore, developing EDA tools with suitable models is essential for advancing these novel technologies.

A. Circuit and Architecture Challenges

The lack of dense memory in superconductors limits the choices for the architecture. In particular, conventional architectures with separate memory and processing units are costly. This forces the designers to reuse memory resources, distribute the memory across the processing units, avoid cache and random access memory in favor of shift registers, and use structures with deep pipeline data streams [16].

SCE logic, such as RSFQ, is a fine-grain pipelined circuit. Hence, in a traditional single-clock synchronous design, all the inputs to each logic level should be path-balanced. This requires the insertion of many path-balancing buffers, in this case, D-Flip-Flops, that incur significant area and power overheads. DFFs are the majority of the gate count in RSFQ logic [17] and can take up 90% of the circuit area in AQFP [18]. The other challenge is that the restriction on fanout requires the insertion of pulse splitter circuits, which increases delay and makes the circuit bulkier. Any signal line needs a distribution tree, and this problem becomes more severe with signals like clocks that require a large distribution network.

The scale of the chips, fabrication limitations, and the need for high current bias prevent designing large-scale circuits on one chip block. Therefore, the developed architectures must decompose the data and operation into multiple smaller blocks. This allows the system to work on multiple chip modules (MCMs) or similar blocks on separate bias islands to incorporate current recycling.

B. Design, Synthesis, Verification, and Testing Challenges

The unique characteristics of SCE introduce challenges at every stage of the design process, including synthesis, verification, and testing.

Fine-grained pipelining impact on design and synthesis. Path-balanced SCE circuits have high latency regarding the number of clock cycles from input to output but enable increased throughput via fine-grained pipelining. In particular, new inputs can be applied to the circuit in every clock cycle, with all logic cell inputs synchronized to the same level. For sequential circuits with loops, new input patterns must synchronize with the circuit's previous state, requiring equal lengths for all internal loops [8]. The fine-grained pipelining in sequential circuits can still support increased throughput, but only in the form of multiple threads of computation, which

must be supported by the EDA flow [19] and the overall design architecture. Moreover, distributing a clock to many clock sinks is a significant challenge. Traditionally, an H-tree design is used to minimize clock skew with a row-based cell placement method [20] in which all RSFQ cells have equal height. RSFQ routing, akin to CMOS, can employ channel-based routing [21].

Fine-grained pipelining impact on timing and verification. In SCE pipelines, the combinational (non-clocked) components include only the interconnects and splitters between consecutive stages of the clocked logic cells. The consequence is that a logic cell whose output fans out to many cells requires many levels of splitters, thus incurring an increased delay. If this increase exceeds a specified target, DFFs can be inserted to add another pipeline stage and cut the splitter tree. A second consequence of the relatively small unclocked components is that the SCE clock period is much more vulnerable to process variations than CMOS, where the variations across many levels of logic gates in combinational blocks reduce the variance of block delays. To address this vulnerability to variations, a statistical timing analysis method has been developed to optimize the clock period [22]. Despite these EDA advances, traditional SCE designs are more susceptible to hold violations, which, like in CMOS, make the chip inoperable and must be fixed before tape-out by conservatively adding hold buffers [23].

Pulse-based operation in SFQ circuits reset their state after processing each input pattern. This lack of memory of the previous states simplifies the delay test for SFQ circuits. Only one test pattern is enough for testing, increasing the delay fault coverage [24]. At the same time, a delay fault in one pipeline level may produce the desired pulse but with extra delay. Such extra delays can accumulate across levels, and after a few levels, the desired pulse can arrive in an incorrect clock cycle. Therefore, the target paths for delay testing must span multiple pipeline levels.

New types of failures occur in SCE due to more complex interactions, fabrication variation, and magnetic and microwave noise susceptibility. An SFQ cell's behavior is influenced by its structure, parameter values, and the cells in its direct fanin and fanout. In addition, signal reflections can occur in the interconnects. In conjunction with the complex interactions and the new operation mechanisms for JJs, process variations cause new types of failures that go far beyond the traditional stuck-at-fault faults. These create new challenges for fault simulation and test generation.

Power consumption and heating. While SCE logic is power efficient and the superconductor doesn't consume DC power, the static power consumption in SFQ logic cells occurs in the bias lines and distribution network. It is not influenced by the logic values applied to the circuit. In contrast, AQFP logic has no bias network; hence, the power consumption depends on the logic value. Therefore, each type of logic has different power considerations. We have developed power analysis tools that consider these factors. For AQFP, similar to CMOS, our power analysis tool uses Monte Carlo-based methods.

C. Integration Challenges with Conventional Technologies

SCE logic needs cryogenic temperatures to work. Conventional SCE logic works at 4.2 K, which is the liquid helium temperature. Keeping circuits at such temperatures requires either He^L or a cryocooler environment with radiation shielding, vacuum conditions, and magnetic shielding [25]. Furthermore, SCE voltage output is high frequency and low amplitude and needs significant amplification. These conditions make interacting with SCE complicated. This requires costly special equipment to test SCE circuits.

Conventional CMOS circuits' characteristics change significantly at cryogenic temperatures, and no accurate models are available in such conditions. Therefore, we must bring the signals to and from SCEs using long wires. The wires should have low thermal conductance to avoid thermal load, be non-magnetic, and have a high-frequency response with low impedance. All these conditions make wiring across large temperature gradients costly. The amplifiers should have a very high gain bandwidth to provide high amplification at RF frequencies. Therefore, adding errors due to delay and noise on the lines, losing data due to amplifier response, and bringing the thermal load to the cryogenic stage are unavoidable [26]. Any architecture, circuit, EDA tool, and testbed should consider all these conditions.

IV. Recent Advances and Unexplored Frontiers in EDA for Superconducting Logic

A. Addressing Clocking and Timing Challenges

The timing challenges of superconducting devices require research into methods that can reduce area and clock overheads, as well as reduce the susceptibility to timing violations.

Clock periods can be reduced by time-borrowing between consecutive blocks and developing a timing analysis method to minimize the clock period. By incorporating time bleeding [27], the value of setup time at the input of a cell can be somewhat decreased, provided we increase the clock-to-Q delay at its output. In addition, dual clocking methods [17], [28] have been developed where one slow clock and one fast clock can be utilized to remove all path-balancing DFFs. The fast clock is used to repeat and propagate data throughout the logic until the valid solution stabilizes at the output, which is captured by a slow clock cycle. The throughput becomes inversely proportional to the logical depth of the circuit when no path-balancing buffers are inserted, although partial path-balancing can increase this throughput. This work has also recently been extended to support multi-threading of sequential circuits [28].

Another means of path balancing without buffer implementation is to utilize multiple clock phases to control data flow through an approach known as multi-phase clocking (MPC). MPC can reduce the number of needed DFFs that is a function of the number of applied phases, i.e., with two clock phases, the drop is 55%, and with ten clock phases, the DFFs saved are 95.5% [29]. The achievable throughput in this method is inversely proportional to the number of clock phases. [30] has shown an efficient approximation of the optimal solution as a linear program that scales to solve phase assignments for

large circuits. Moreover, recent developments have extended multi-phase clocking to ensure a hold-safe solution such that any hold-time problems can be fixed post-fabrication [19], [30]. This is accomplished by ensuring connected gates have differing clock phase assignments, enabling fixing any hold violations by increasing the skew between clock phases. However, these novel clocking methodologies still need to be improved with support for targeted tech mapping, clock tree synthesis, and supporting place & route tools. Another recent work has combined multi-phase clocking and gate compounding [31] to demonstrate an average reduction in JJ count of 59% over dual clocking methods alone when achieving the same throughput. The demonstrated benefits of utilizing both gate compounding and multi-phase clocking create the opportunity to develop optimization algorithms for this new scheme and suggest combinations of multiple clocking schemes that need to be further explored by the superconducting EDA community.

In AQFP logic, in contrast, synchronization is achieved via AC biasing, and splitters are clocked circuit elements. Novel clocking methods such as AQFP N-Phase clocking [32] and delay-line clocking [33], [34] can improve integration by allowing for connections between logic elements of non-adjacent phases, known as phase skipping. Joint buffer and splitter insertion optimization with phase skipping was recently proposed, showing 48.6% average savings in buffer and splitter insertion when skipping one phase and 70.3% when skipping three phases [35]. Optimization methods using N-Phase clocking show benefits over other buffer/splitter insertion methods and are a new area that needs further exploration.

B. Addressing Testing and Verification Challenges

We have developed a new automatic test pattern generator (ATPG) for delay faults [24], [36]. It targets paths that span multiple pipeline levels and selects paths based on RSFQ-specific characteristics to dramatically reduce the complexity and cost of delay testing and yet improve fault coverage.

We have developed a new comprehensive cell verification and characterization method [37], which thoroughly verifies the cell behavior by enumerating all possible configurations for each cell under study (CUS), including all possible cells and interconnects in its fanin and fanout. To derive fault models, the above framework has been extended to also consider different process variation ranges [38]. Simulations using this framework identify tens of thousands of failures where simulation results have errors relative to the golden results. We have developed Inductive Fault Model Extraction (IFME) [38], a data-driven method which inductively learns a comprehensive set of fault models, including many completely new fault types, from all the above failure data using the labels we assign to a small number of failure instances.

The higher speed and cryogenic operation of superconductive electronics make it impossible to use external test equipment for testing. Hence, design-for-testability (DFT) and built-in self-test (BIST) methods are necessary. However, due to fine-grain pipelining, the existing DFT and BIST methods cannot be used for RSFQ. We have developed new DFT [39] and BIST [40] methods for comprehensive testing of SFQ logic, including at-speed testing.

C. Addressing multi-threading

With the various degrees of path balancing and fine-grained pipelining, superconducting logic naturally supports multi-threading [29]. However, efficient architectural management of the various threads must be considered, and in many applications, each thread must have independent storage. This emphasizes the need for efficient memory cells and multi-threaded memory in SFQ devices. Recent work [41] has utilized pipelined register files to support multiple threads, but such work needs further development.

D. Improving Integration

Improvement in timing synthesis verification tools and clocking methods helps with large circuit implementation and enables handshakes between different chips and cold head and room temperature devices. This will prevent data loss and reduce error while maintaining the high performance of SCE. The high bias current value is addressed by modifying the circuits for new biasing paradigms like SFQ biasing [42]. The AC or SFQ biasing has no static power consumption and is less thermally costly to transfer. However, the cost of transformers should be included in the circuit budget for these methods.

In the NSF-funded Expedition: DISCoVER project (see discoverexpedition.usc.edu), we are working on improving the integration of SCE by using MCM encompassing different architectures, such as neuromorphic, Ising machine, CPU, and memory core. Each task will be assigned to the core based on the arbitrator circuit. The combination of architecture, packaging, and data communication methods results in maximum performance out of SCE circuits. Interfacing SCE logic with each other and conventional technologies needs high-performance amplifiers, which is an issue in high interconnect numbers. This issue is addressed by implementing a preamplification stage with SCE logic. The amplification is done with a Suzuki or SQUID stack [43] and has a high bandwidth with low noise. Preamplification reduces the cost of amplifiers and the chance of data loss on wires.

V. Conclusions

Superconductor electronics is a promising technology with many challenges. Moving beyond CMOS with SCE logic requires scaling up the circuits and making them more accessible. We have addressed several challenges in the architecture, circuit design, fabrication, and integration of SCE logic and how they affect the performance and feasibility of this promising technology. While these challenges are being addressed, much room exists for improvement.

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