Trans-Net: Knowledge-Transferring Analog Circuit Optimizer with a Netlist-Based Circuit Representation

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***Abstract*—Finding an optimal point in the design space of analog circuits requires a substantial time-consuming effort even for skillful circuit designers. There have been extensive studies on automated sizing of transistors in analog circuits based on machine learning (ML) algorithms. However, the previous approaches suffer from lack of expandability and necessitate an inevitable retraining process of the given model to apply for optimization of different circuits. The graph-based representation of a circuit with reinforcement learning (RL) achieved a knowledge transfer when optimizing the same circuit with different process technologies. However, it can be hardly applied to different circuit topologies due to the failure of generalizing the training of RL agent. This paper introduces Trans-Net, an analog circuit optimizer that is capable of supporting the knowledge transfer across different circuits as well as different process technologies with a circuit representation that defines the circuit topology by one-to-one mapping from SPICE netlist. The proposed analog circuit optimizer successfully supports multiple circuits within a single ML model, showcasing its effectiveness on five different circuit topologies across three different process technologies.**

***Index Terms*—analog circuit optimization, design automation, transfer learning, transistor sizing, reinforcement learning**

I. Introduction

Optimization of analog circuits in a vast design space demands a significant time and the highest level of engineering expertise. Researchers have explored automated techniques for transistor sizing using machine learning (ML) algorithms. While these approaches have shown effectiveness in optimizing single circuits, they suffer from lack of expandability to different circuits, necessitating repeated retraining of the same model for each new circuit optimization task.

Researchers have explored embedding a graph-based circuit representation [1], [2] in reinforcement learning (RL) for knowledge transfer. The graph-based circuit representations use an adjacency matrix (A) for connectivity and a feature matrix (X) for devices details. However, the GCN-RL [1] neglects the node-level connectivity for differentiating gate, drain, and source of each MOSFET. Though CAN-RL [2] realizes an one-to-one mapping between adjacency matrix and the circuit, the processing for embedding devices to the adjacency matrix (AX) destroys the one-to-one mapped representation of the circuit (Fig. 1). This failure of one-to-one representation eventually limits the effectiveness of graph-based methods in transfer learning.

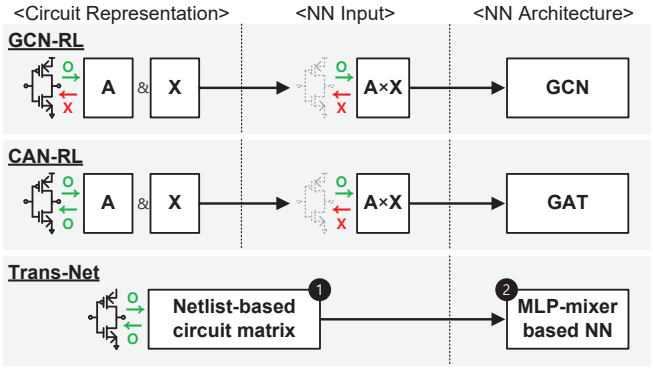

Fig. 1: A brief overview of GCN-RL, CAN-RL and Trans-Net.

This paper introduces Trans-Net, an analog circuit optimizer that circumvents the problems of the knowledge transfer across disparate circuits and process technologies. Our work includes two key-enabling schemes as shown in Fig. 1:

1. We introduce a compact circuit representation with one-to-one mapping in a way of SPICE netlist description, enabling a direct processing of the raw input at the first layer of the critic network. It eliminates extra processing for embedding the adjacency matrix required in graph-based networks.
2. We propose an MLP-Mixer-based neural network architecture tailored for the processing of netlist-based circuit matrices, encompassing both device and node information.

II. Trans-Net

Fig. 2 provides an overview of the proposed netlist-based analog circuit optimizer (Trans-Net). A netlist typically encompasses three types of information (Fig. 2a): device, node connectivity, and feature parameters for each device. this netlist is directl mapped into a matrix, wherein each row of the matrix corresponds to an individual row of the netlist. The columns of matrix representation can be partitioned into three sub-blocks, each corresponding to a different type of information in the netlist. The first sub-block indicates the type of device, which is encoded using one-hot encoding. The second sub-block represents node connectivity information by assigning $'0'$, $'1'$, and $'-1'$. The last sub-block informs

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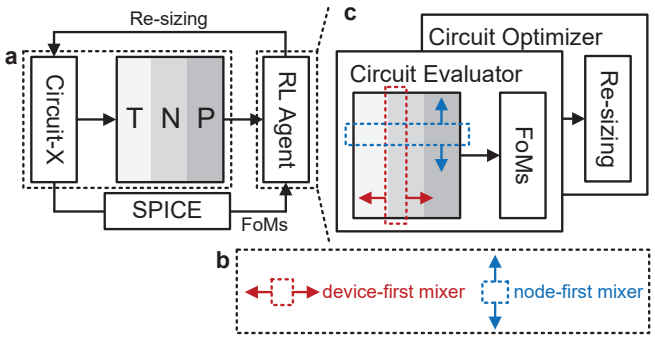

Fig. 2: A brief overview of Trans-Net.

parameters of each device. The size of the matrix defines the maximum number of devices and nodes. The unused rows and columns are padded with zeros for smaller circuits.

We adopt the processing of the MLP-Mixer [3] to fuse these two forms of circuit information. The mixer layer comprises two sub-blocks (Fig. 2b): the device-first mixer and the node-first mixer. The device-first mixer initially aggregates device-wise information. Subsequently, it transposes the intermediate output, conveying the aggregated device-wise information in a node-wise manner. Conversely, the node-first mixer starts by aggregating node-wise information.

Two distinct parts, the circuit evaluator (CE) and the circuit optimizer (CO), are shown in Fig. 2c. The CE, which is similar to critic network, estimates the figure of merits (FoMs) of the circuit by executing a resize action for a given circuit state. The objective of the CE is to minimize the difference between the predicted FoMs and the actual FoMs. The CO, which is similar to actor network, generates a desired action for a given circuit state. The CO is trained to maximize the FoMs of the circuit.

III. Experiments

The training phase aimed to empower the circuit agent with the capability to maximize the FoM, Eq. (1), while simultaneously ensuring the PM of a minimum of 60 degrees.

$$\text{FoM} = \frac{\text{GAIN (dB)}}{70\text{dB}} + \frac{\log_{10}(\text{GBW})}{\log_{10}(1\text{GHz})} - \frac{\log_{10}(\text{Power})}{\log_{10}(1\text{mW})} \quad (1)$$

Fig. 4 presents the average FoM of Circuit-E in the 45nm process while progressively adding knowledge from more circuits, depicted in Fig. 3. Simulated 100 data points were prepared as the knowledge for each circuit, denoted as D_A, D_B, D_C, D_D, and D_E. When referring to *All D*, it encompasses the complete datasets, including 5 circuit topologies across TSMC 45, 65, 180nm technologies (1500 data points in total) with HSPICE. Differing from GCN-RL and CAN-RL, as the amount of data for training increases, no matter what circuit the data are obtained from, the Trans-Net consistently improves its performance. In all three cases, the learning approach uniformly adheres to the DNN-Opt [4] framework.

IV. Conclusion

Previous ML approaches for transistor sizing have limitations in expandability and adaptability due to the constraints of graph representation. Trans-Net, an analog circuit optimizer, enables knowledge transfer by mapping SPICE netlist topology and successfully optimizes five circuit topologies across three process technologies within a single machine learning model.

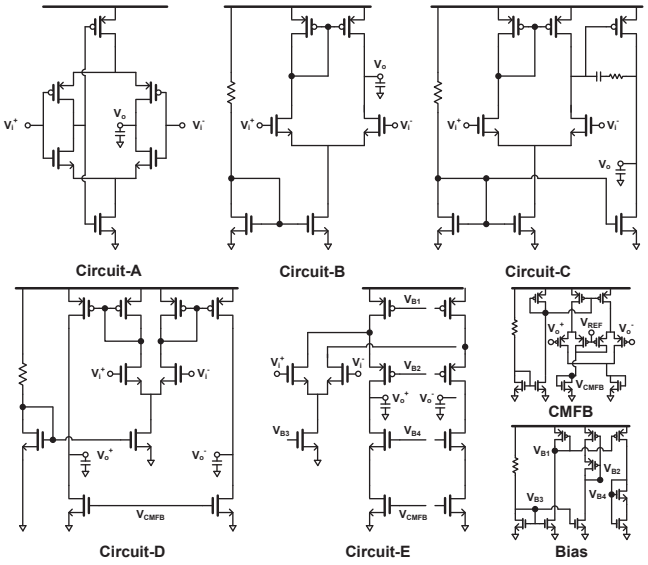

Fig. 3: Five diffrent circuits.

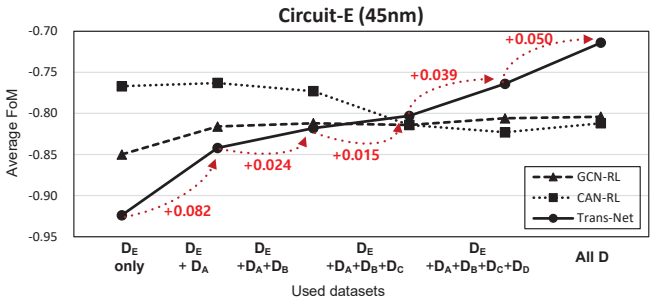

Fig. 4: The impact on knowledge transfer across topologies when transferring knowledge to Circuit-E with 45nm.

Acknowledgment

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