Dynamic Reconfigurable Security Cells based on Emerging Devices Integrable in FDSOI Technology

Niladri Bhattacharjee[1], Viktor Havel[1], Suruchi Kumari[2], Nima Kavand[3], Jorge Navarro Quijada[3], Akash Kumar[3], Thomas Mikolajick[1,2] and Jens Trommer[2]
[1]NaMLab gGmbH, Nöthnitzer Str. 64a, 01187 Dresden, Germany
[2]Chair for Nanoelectronics, TU Dresden, Nöthnitzer Str. 64, 01187 Dresden, Germany
[3]Chair of Processor Design, TU Dresden, Helmholtzstraße 10, 01062 Dresden, Germany

***Abstract*—While a number of measures have been proposed to protect the integrity of COS hardware, there are some inherent limitations from classical CMOS methods. Those already existing security methods, like logic locking can be improved with emerging technologies such as Reconfigurable Field Effect Transistors (RFETs). RFETs are a special type of doping-free, Schottky transistors which can work as a PFET or NFET as a function of biasing across its gates. In the present study we developed standard cell layouts for dynamic reconfigurable security cells based on three-independent-gated RFETs (TIG-RFETs). They layouts are compatible to an industrial 22nm FDSOI technology, feature the minimum pitch of the baseline technology, and obey all design rules necessary for co-integration. The designs enable a fair area comparison for RFET based digital application for the first time. Based on the sizing constraints from the layouts, a TCAD model of such a TIG-RFET is developed in Sentaurus TCAD to illustrate two biasing schemes for the application of TIG-RFETs in this platform: reconfigurability with individual body-bias per transistor and reconfigurability at globally fixed body-bias. Due to the different operation options three variants of reconfigurable 2-XOR-XNOR and 2-NAND-NOR logic cells exhibiting different level of utility are designed. While the smallest dynamic 2-NAND-NOR gate needs roughly double the area of a CMOS 2-NAND gate from the reference library, the smallest 2-XOR-XNOR gate is only 20% larger than a CMOS 2-XOR. To quantify the area overhead for hardware security applications we calculated the number of logic locking gates that can be added per area overhead for a given circuit, here the ISCAS-85 C6288 benchmark circuit, as an example. Dynamic replacement based logic locking with TIG-RFETs shows to allow up to double the number of keys compared to classical CMOS logic locking per area overhead. Therefore, this work allows a realistic view on the application of RFETs in hardware security and its co-integrability along with some design constraints from an industrial PDK.**

***Index Terms*—Hardware security, Reconfigurable FETs, TCAD modelling, Standard Cell Designs, Design-Technology-Co-Optimisation, Design-For-Manufacturability**

I. Introduction

Coping with the growing need to improve the capability of electronic systems, there is an upcoming trend to consider emerging technologies that allow new device functionalities. Such emerging trends allow innovative circuit applications, especially in areas where CMOS have their limitations. One of these areas is hardware security. Classical CMOS devices are inherently weak against attacks on the hardware level due to their underlying differences in doping, channel materials and geometry. Reconfigurable field effect transistors (RFETs) are such an emerging technology, which address these security vulnerabilities effectively. They allow seamless switching between PMOS or a NMOS functionalities and are characterised by their doping-free nature, utilising metallic contacts at the source/drain to form Schottky barriers. A multitude of independent gates can be used to control the type of carrier injected into the channel. Various structures of RFETs have been proposed in the past such as Back-Bias RFETs [1], Three-Independent-Gate RFET (TIG-RFETs) [2], Multiple-Independent-Gated RFETs [3], as well as disruptive cross-shaped structures with multiple source/drain contacts [4]. RFETs are especially promising for co-integration with CMOS, as they share all needed materials and process steps with the baseline technology. Among potential technologies for RFET co-integration, an application as an add-on into fully-depleted-silicon-on-insulator (FDSOI) platforms has gained the most attention [5], [6]. For bulk technologies, an epitaxial selective overgrowth technique has been proposed enabling RFETs on a local SOI area [7]. Applications of RFETs span a wide range, from analog uses like differential amplifiers [8], to digital applications for constructing adaptable logic functions aimed at enhancing hardware security [9]–[12]. In this study, we have developed standard cells for dynamically reconfigurable logic functions based on Three-independent-Gated RFETs (TIG-RFETs), that are intended to be co-integrable with CMOS. The work is focused on a design-technology co-optimisation (DTCO) study around the two most prominent designs for hardware security: the 2-NAND-NOR and a 2-XOR-XNOR dynamic logic gates. All layouts presented are clean against the core design rules of industrial 22 nm FDSOI platform [13], thus allowing for a fair area comparison for the first time. We will show that the influence of the applied back-bias inherent to the FDSOI technology has a high impact on both the device characteristics and on

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the cell to be used in each application scenario.

The remainder of the paper is organised as follows: Section II introduces TIG-RFET transistors integrable into a 22 nm FDSOI platform. Two biasing schemes originating from the nature of the SOI platform are discussed. Section III presents the developed standard cell layouts of the dynamic logic functions. Their corresponding benefits and disadvantages related to the employed biasing scheme are discussed. An area comparison to a classical CMOS reference library is given. Section IV illustrates different options for employing those standard cells for digital design embedded into CMOS. Some manufacturability constraints and potential impacts on place-and-route during the EDA process are briefly discussed. Finally, in section V, the potential benefits of dynamic replacement-based logic locking technique with RFETs is compared to classical additive CMOS logic locking, which is exemplified on an ISCAS-85 benchmark circuit. Our work provides the first realistic projection of the advantages of TIG-RFET based dynamic logic-locking, derived from an industrial platform.

II. Biasing Schemes for TIG-RFETs on FDSOI

For the analysis in this paper, we have opted for the 22FDX technology from GlobalFoundries as our baseline technology [13]. The technology has shown to be able to facilitate RFETs with equal N- and P-current, which are programmed by the unique feature of applied back-bias [1], [5]. The back-bias needed to program to the devices is typically 3-5 times higher than the nominal V_{DD}. However, a single operation voltage is typically desired to achieve dynamic reconfigurable in digital applications. This can be achieved using three independent gate electrodes at the front-side [2]. Layout and cross-sectional structure of such a TIG-RFET device are shown in Fig. 1a) and b) respectively. We considered all technological constraints 22 nm baseline technology [13], [14], including minimal gate length and contacted poly pitch. The outer two gate electrodes are aligned with the silicide contact at the source (source gate, SG) and drain (drain gate, DG), while the central gate (CG) steers the centre of the channel. Depending if the transistor is operated at SG (CG), the device exhibits a high V_T (low V_T) behaviour. The DG potential is used to block the undesired carrier type and yields the program of the devices. In the case of an FDSOI technology, an additional back-gate (BG) contact has to be considered, influencing the channel from the back side. The influence of adaptive-body-biasing in FDSOI [15], [16] was analysed in Sentaurus TCAD for two use cases of reconfigurability: first, an individual back-bias for P- and for N-mode and second, a fixed back-bias bias for both modes. In the TCAD model, source/drain contacts were set to be Schottky and for the undoped silicon, auger recombination, high-field saturation and transverse field dependence (Enomral) mobility models were enabled during the simulations. For the symmetry of the P- and N- ON-currents, for both the cases, the following fitting parameters were used: 4.56 eV gate-metal work function (W.F.), 4.7 eV for source/drain W.F., $0.12m_o$ and $0.134m_o$ effective masses for the electron and holes respectively.

In Fig. 1b), the transfer characteristics for the first biasing scheme are shown. Here, the individual program voltage applied at the DG is also applied at the BG for P- and N-mode. During the N-operation mode, the BG is biased at V_{DD} and during the P-operation, the body is biased at the ground. The BG voltage is thereby dynamically contributing to the reconfigurability. This mode of biasing ensures equal potential difference between the device's body and source/drain terminals for the P- and N-modes and yields a symmetric operation with our parameter set.

For the second case displayed in Fig. 1c), at a fixed bias across BG (V_{BG}), the programming of P- and N-functionality is only realised by the DG potential. The fixed BG voltage is again chosen so that the maximum on-currents for N- and P-mode are identical and can be coupled with the CMOS transistors. For this use case, the ON-currents are smaller than the back-bias as a program-gate. Albeit this implies individual worse device performance compared to the other biasing scheme, we will show in the next section that the feature will enable a distinct area reduction of the underlying standard cells.

III. Layouts for Standard Cell Design

In this section, standard cell layouts for the dynamic reconfigurable cells based on the constraints of the 22FDX^{TM} [17], platform are discussed. The importance of the two, device-level BG biasing schemes are highlighted. We focus on the two most relevant designs for hardware security applications: a dynamic 2-NAND-NOR gate and a dynamic 2-XOR-XNOR gate.

Fig. 2a) depicts a schematic of the reconfigurable 2-NAND-NOR cell capable of switching between a 2-NAND or a 2-NOR configuration based on the input signal P. All TIG-RFETs in this circuit have the same bias across their BG. This circuit is an illustrative example of reconfigurability while keeping at a fixed back-gate voltage for all TIG-RFETs. Complementary, Fig. 2b) showcase a four-transistor arrangement for a 2-XOR-XNOR logic gate, which can execute either 2-XOR or 2-XNOR as a function of the input signals P. Notably, the TIG-RFETs in the pull-up and pull-down sections are biased to different back-gate voltages. This configuration exemplifies the individual back-bias scheme, wherein the bias across the BG of each TIG-RFET is in conjunction with the program signal P or $\bar{\text{P}}$ of the respective network. The related standard cells are discussed in the following.

Simplified layouts of all discussed standard cell versions are displayed in Fig.3. Note that all 2-NAND-NOR (2-XOR-XNOR) gate versions are built on the same static core. If this core alone is used, it can be seen as the static equivalent of only half its functionality, where the programming has to be executed via the metal lines. Due to the higher number of poly-gates, the area overhead in this static case is quite large. However, to fully enable dynamic reconfigurability of each standard cell, close-by CMOS inverters and the necessary intra-cell, metal-layer(s) wirings were added. Each resulting cell comprises all the inverters necessary for the input input

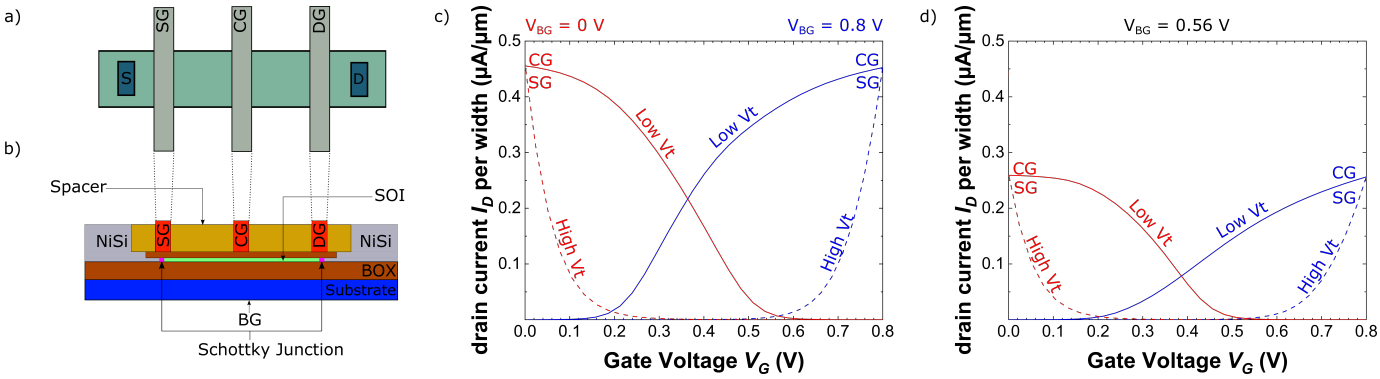

Fig. 1. Biasing Schemes for TIG-RFET built on an FDSOI baseline technology. a) The layout of a TIG-RFET model based on the minimum design rules of the baseline technology. b) Cross-sectional view of the corresponding TCAD model. c) P- and N-mode transfer characteristics of the modelled TIG-RFET including the multi-V_T operation after steering at SG (high-vt) and CG(low-vt). The back-gate is biased at the same level as the DG in each of the modes. d) Transfer characteristics of the same device, if the back-gate is kept at a common fixed bias of 0.56 V (V_{BG}), which enables symmetry for both the modes.

TABLE I
AREA OF TIG-RFET STANDARD CELLS SHOWN IN FIGURE 3 AND COMPARISON WITH CMOS CELL REFERENCE IN THE SAME TECHNOLOGY. AREA RATIO IS GIVEN WITH RESPECT TO STATIC 2-NAND OR STATIC 2-XOR, RESPECTIVELY.

Biasing Scheme	Individual Back-Bias (with Well-Taps)		Fixed Back-Bias (Tapless)		
Use Case / Logic Function	Static RFET core area | Area ratio to static CMOS counterpart	Dynamic RFET cell area | Area ratio to static CMOS counterpart	Static RFET core area | Area ratio to static CMOS counterpart	Dynamic RFET cell area matched with CMOS height | Area ratio to static CMOS counterpart	Dynamic RFET cell area with minimal height | Area ratio to static CMOS counterpart
NAND/NOR	2.94 µm² | 2.31	4.51 µm² | 3.53	1.97 µm² | 1.54	3.27 µm² | 2.56	2.65 µm² | 2.07
XOR/XNOR	2.94 µm² | 0.95	6.48 µm² | 2.09	1.97 µm² | 0.63	4.75 µm² | 1.53	3.84 µm² | 1.23

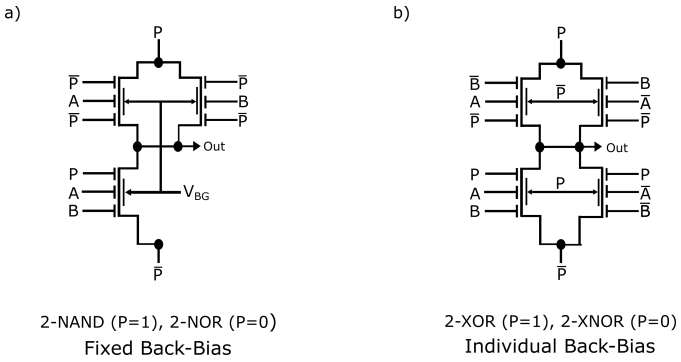

Fig. 2. Dynamic Reconfigurable Logic Gates. a) Schematic of a 2-NAND-NOR reconfigurable cell, that can be programmed as 2-NAND (P=1) or 2-NOR (P=0). The Back-Gate (BG) of each of the TIG-RFET is biased at a fixed voltage of V_{BG}. This is an example of reconfigurability at a fixed Back-Bias b) Schematic of reconfigurable 2-XOR-XNOR, which can function as a 2-XOR with TIG-RFETs (P=1) and 2-XNOR (P=0). The pull-up and pull-down networks have a different biases at the BG i.e. they have individual back-Bias. This is an example of BG contributing to reconfigurability.

signals along with the TIG-RFETs. A common program signal (P) is used to select the required functionality of the logic gates. The presented cells are clean against the core design-rule-checks and intended to be co-integrable with classic CMOS standard cells. These standard cells allow an area comparison with our self-designed CMOS reference library, giving an idea of the area overhead needed by these cells. Table I summarises the area of our TIG-RFET standard cells. Fig. 3a), c) and e) show the standard cell layouts for the 2-NAND-NOR, while Fig.3b), d) and f) show the layouts for the 2-XOR-XNOR. The layouts shown in Fig. 3a) and b) have local well-taps for each TIG-RFETs, i.e. they are targeted for the biasing scheme with independent back bias. The 2-NAND-NOR and 2-XOR-XNOR are 3.53 and 2.09 times larger than the CMOS equivalents, respectively. These local-well-taps logic cells are 1.36 and 1.69 times larger than the tap-less cells with the CMOS and TIG-RFET heights, respectively. Therefore, the device has the highest area overhead in this scheme, thus trading performance for the area. Fig. 3c)-f) are tap-less, meaning that the common well is shared for all TIG-RFET blocks and is intended for the fixed-back bias scheme. We placed the TIG-RFETs typically onto the same well as the N-MOS transistor of the related inverter circuits [15]. The standard cells shown in Fig. 3c)-d) still, obey the height constraints from the CMOS reference. In this case, the reconfigurable 2-NAND-NOR are about 2.56 times larger than the 2-NAND cell, whereas the reconfigurable 2-XOR-XNOR is 1.53 times larger than a 2-XOR. It is also possible to further reduce the height and consequently the area of the cells by means such as an optimised routing of the metal lines such as shown in Fig. 3e) and f), where the metal line M2 is routed over the active region of the transistor, leading to a height reduction of the standard cells from 1.68 µm (CMOS matched) to 1.36 µm (minimal

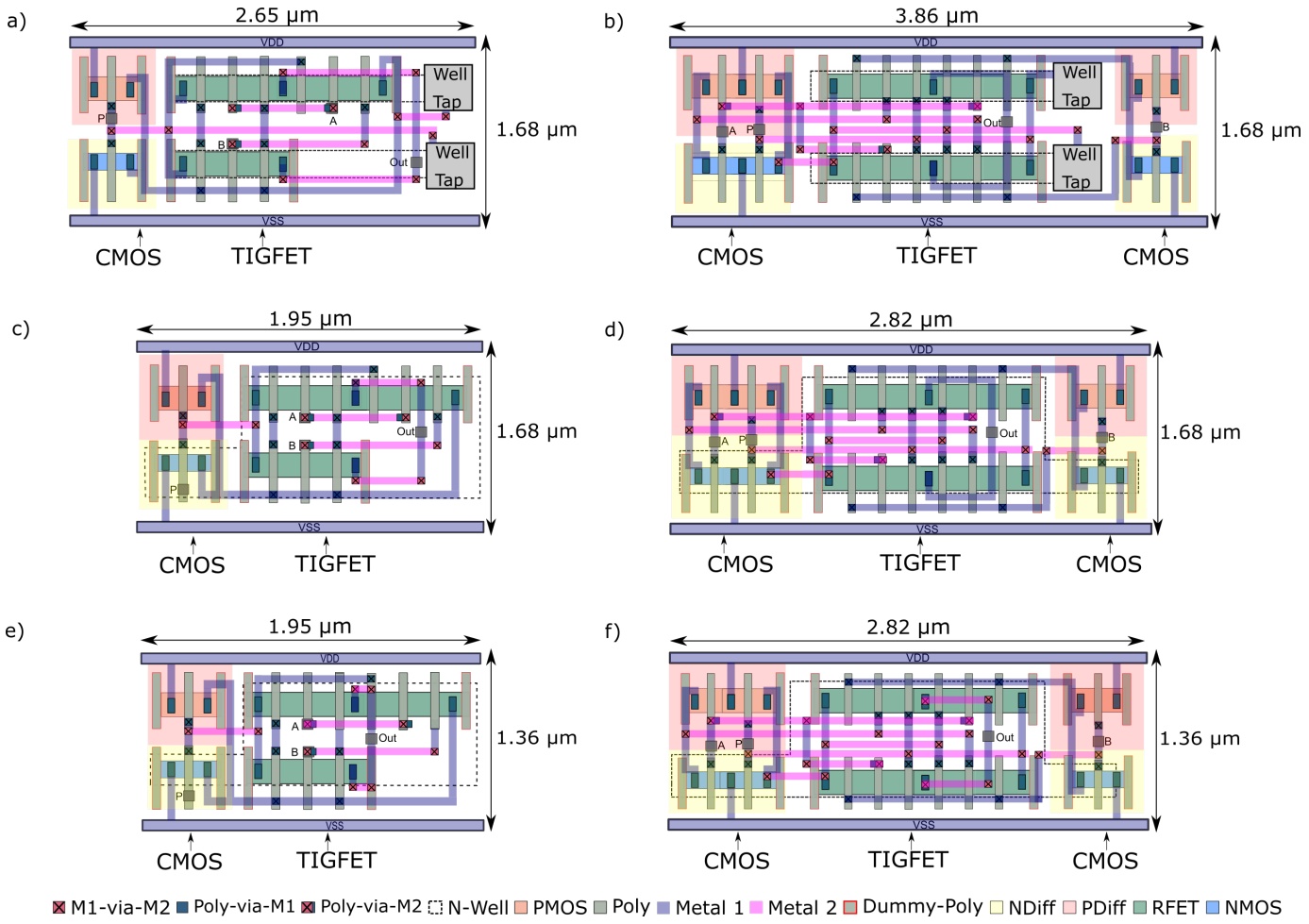

Fig. 3. Standard Cell Layouts for Hardware Security Cells: a)-f) show the simplified layouts of a reconfigurable 2-NAND-NOR and 2-XOR-XNOR cells respectively. a) and b) shows the layout of a 2-NAND-NOR and 2-XOR-XNOR cell, respectively built in different wells and have local well-taps. The well-taps provides the biasing necessary for the scheme of individual back-bias for programming the TIG-RFET. c) and d) shows the layouts for the reconfigurable 2-NAND-NOR and 2-XOR-XNOR, respectively, where the designs are tap-less. Here the biasing scheme of a common fixed back-bias can be applied. The wells of the TIG-RFETs and NMOS are shared. The cells are designed with the height of the CMOS reference library. e) and f) show the smallest layouts of the reconfigurable 2-NAND-NOR and 2-XOR-XNOR. Here, M2 is routed over the active region of the RFET reducing the cell size to the minimal possible height.

TIG-RFET height). This enables a further area optmisation and allows the possibility of transistor scaling in width to match the CMOS reference heights. Here, the 2-NAND-NOR and 2-XOR-XNOR reconfigurable cells are 2.07 times and 1.23 times larger than the CMOS cells. Only the layouts in Fig. 3a, b) enable the higher on-state performance as provided by the independent back-bias scheme. It becomes a trade-off between a larger area overhead and higher performance compared to the other cases. Note that for all these layouts, conventional design methods obey the design requirements for manufacturability (DFM). The power rails for these TIG-RFET-based logic functions are kept similar to the power rails of the CMOS cells, i.e. above and below the cells for an easier place-and-route in the future development of the EDA flow around it. This may lead to higher parasitic, as compared to earlier TIG-RFET layout approaches, where power rails are placed orthogonal with different metal layers [18]–[20], but enables easier co-integration with CMOS designs. The designs are clean against the design rule checks and limited by the need for measures for protecting the un-gated regions from all other process steps and keeping the TIG-RFETs doping-free. Following the conventional layout approach also has the benefit of structurally securing the obfuscated logic gate by camouflaging [21].

IV. Discussion of Physical Synthesis Peculiarities

Contrary to the CMOS transistors, where the NMOS and PMOS transistors are in complementary nets, the TIG-RFETs structurally mimic each other in both the pull-up and pull-down networks. However, from a functional standpoint, they still perform complementary operations. As already discussed before, in Fig. 3a) and b), the TIG-RFET blocks have local well-taps while the well-taps for the CMOS inverters are assumed away from the cell design, i.e. the CMOS blocks

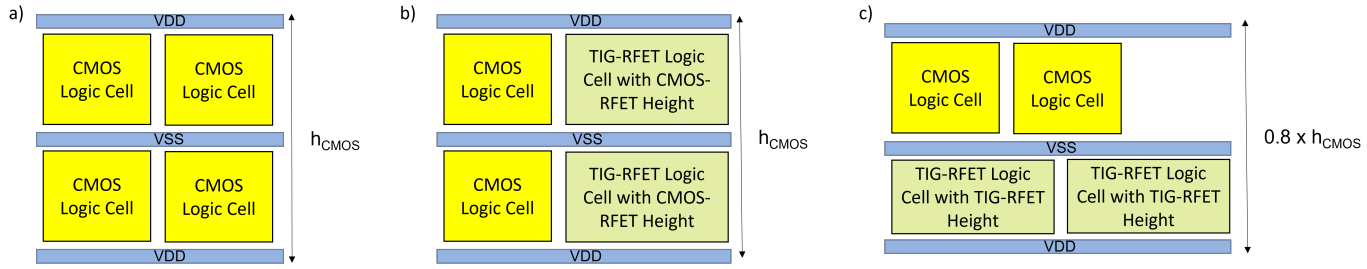

Fig. 4. Example of Physical Synthesis Applications. a) During Place-and-Route, CMOS logic blocks are arranged in a grid with a total height of h_{cmos} for the netlist b) TIG-RFET reconfigurable logic cells can be arbitrary placed next to CMOS cells. TIG-RFET cell height has to obey CMOS height, to ensure straight power rail distribution. c) TIG-RFET cells with minimal height, when placed in a individual row during place-and-route, reduces the total height by a factor of 0.2. This leads to higher constraints on the place-and-route effort during physical synthesis.

can share their taps across tap-cells but not for the TIG-RFET blocks. The body biasing is different for the pull-up and pull-down networks, corresponding to the argument that the pull-up and pull-down blocks cannot share the wells they are built in. Contrary to the individual Back-Bias case, for reconfigurability at a fixed bias, the pull-up and pull-down networks may or may not share the wells. The example of the TIG-RFETs sharing their well has been demonstrated in Fig. 3c)-f). The RFET blocks can also share their wells with the corresponding NMOS blocks. The well-taps are assumed to be away from the cell designs for the TIG-RETs and the CMOS, i.e. in dedicated tap-cells, and can thereby share their body bias with other CMOS transistors. Horizontally, the width of the cells is limited by the gate-pitch. The two different heights of the cells (matched to CMOS cell height and minimal TIG-RFET height), under consideration in the present study, lead to two application cases in a grid-based circuit place-and-route scheme for larger circuits. An example illustrating such a grid-based place-and-route of different CMOS is shown in Fig. 4a). The TIG-RFET-based reconfigurable cells with the CMOS heights can, therefore, be placed randomly with the CMOS cells without changing the power-rail pitch of the CMOS logic cells, as is illustrated in Fig. 4b). In our designs, having the TIG-RFET next to the CMOS transistors necessitates a diffusion stop dummy-poly-gate, consequently increasing the standard cell's width. Therefore, larger circuits using such reconfigurable cells in a distributed manner must adapt the dummy-poly-gate constraint, especially when driven over an automatic place-and-route scheme. Alternatively, Fig. 4c) shows that replacing an entire row of CMOS logic blocks with these height-reduced TIG-RFET logic blocks leads to net height of the complete circuit netlist reduction by a factor of 0.2, compared to the case of Fig. 4a). In this case, all RFET cells are placed next to each other, freeing constraints on the CMOS gate designs. However, the complexity of achieving this solution is increased at the place-and-route level, due to the larger placing constraints for the RFET cells.

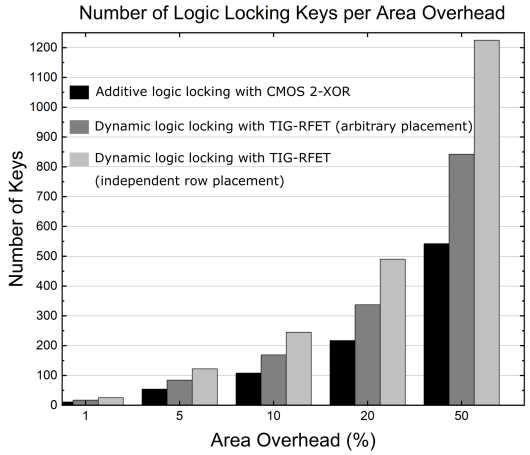

Fig. 5. Comparison of number of logic locking keys with dynamic logic locking using the reconfigurable 2-NAND-NOR compared to the traditional CMOS 2-XOR based logic locking per area overhead for the ISCAS-85 C6288 benchmark circuit. The x-axis represents the allowed area overhead, while the y-axis represents the number of keys which can be added for the corresponding area overhead. Arbitrary placement of reconfigurable 2-NAND-NOR cells is compared with independent row placement of the RFET cells with minimal height.

V. Comparative Analysis of Dynamic Reconfigurable Cells in Logic Locking

In this section, the application of the dynamic reconfigurable cells for a replacement-style lock locking scheme is compared to classical CMOS-based additive logic locking. As an example, this comparison is performed for the C6288 circuit from the ISCAS-85 benchmarks. The number of keys that can be added per area overhead has been calculated by applying the different physical synthesis schemes discussed in Section IV, without considering any constraints from placement algorithms. For the CMOS case of additive logic locking, the area of a static 2-XOR is used for each key. For a 5 % area overhead tolerance, about 54 extra 2-XOR can be added with this technique. For the case of replacement-based dynamic logic locking, we added 2-NAND-NOR reconfigurable cells to replace the 2-NOR and 2-NAND of the original netlist. The use case of arbitrary gate placement utilising cells obeying

CMOS height constraints (TIG-RFET cells matching CMOS heights) is compared with placing all key gates in a single row with minimal height of the TIG-RFET cells, thus saving about 20% of area per cell. Fig. 5 shows that for the first case of arbitrary placement, an average of 1.5 times more keys can be added per area overhead as compared to classical CMOS logic locking. If all TIG-RFET gates are placed in an individual row during physical synthesis, nearly double the number of keys can be added per area overhead. For the 5 % area overhead example, 84 and 122 keys can be added by introducing the TIG-RFET cells, respectively. This scales almost linearly with increased overhead tolerance as illustrated upto a maximum of 50 % added area. Please note that an even higher benefit can potentially be achieved if the benchmark is synthesised in an XOR-rich logic style as proposed in [22].

VI. Conclusion

Dynamic reconfigurable standard cells using three-independent-gate reconfigurable field effect transistors (TIG-RFETs) compatible with an industrial 22 nm FDSOI platform have been presented. Two distinct biasing schemes and two different height options have been explored. The layouts are clean against design rule checks and meet the design for manufacturability (DFM) requirements. While the smallest dynamic 2-NAND-NOR gate needs roughly double the area of a CMOS 2-NAND gate of the reference library, the smallest 2-XOR-XNOR gate is only about 20% larger than the respective CMOS 2-XOR. The benefit of the reconfigurable cells in replacement based dynamic logic locking has been illustrated on an example of a C6288 benchmark circuit. upto double the number of keys could be added for the same overhead area compared to traditional CMOS based logic locking. The work presented here provides insight into the application of TIG-RFETs in hardware security while considering the design constraints for its co-integration within a CMOS technology.

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