# Reinforcement Learning-Based Optimization of Back-side Power Delivery Networks in VLSI Design for IR-drop Reduction

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***Abstract*—On-chip power planning is a crucial step in chip design. As process nodes advance and the need to supply lower operating voltages without loss becomes vital, the optimal design of the Power Delivery Network (PDN) has become pivotal in VLSI to mitigate IR-drop effectively. To address IR-drop issues in the latest nodes, a back-side power delivery network (BSPDN) has been proposed as an alternative to the conventional front-side PDN. However, BSPDN encounters design issues related to the pitch and resistance of through-silicon vias (TSVs). In addition, BSPDN faces optimization challenges due to the trade-off between rail and grid IR-drop, particularly in the effectiveness of uniform grid design patterns. In this study, we introduce a design framework that utilizes reinforcement learning to identify optimized grid width patterns for individual VLSI designs on the silicon back-side, aiming to reduce IR-drop. We have applied our design approach to various benchmarks and validated its improvement. Our results demonstrate a significant improvement in total IR-drop, with a maximum improvement of up to $-19.0\%$ in static analysis and up to $-18.8\%$ in dynamic analysis, compared to the conventional uniform BSPDN.**

***Index Terms*—IR drop, Reinforcement Learning(RL), Back-side Power Delivery Network(BSPDN), VLSI.**

## I. Introduction

On-chip power planning is one of the key processes in 2D chip design, which refers to the process of designing the power delivery network (PDN) to supply the intended power. A pivotal concern within PDN design is the IR-drop, which is the voltage reduction that occurs due to metal or intermetallic parasitic components in the PDN. In VLSI designs, severe IR-drop issues cause power loss and chip degradation. Moreover, modern VLSI chips consume more power, and this exacerbates the challenge of meeting IR-drop constraints [1]. In order to mitigate this IR-drop, designers estimate its amount during the design phase and generate optimal PDNs. Commercial electric design automation (EDA) tools provide quite accurate IR-drop estimates, but they may lead to more design iterations that increase the overall design time if they do not meet the target IR-drop. Also, these tools demand high computational resources for accurate results [2]. Recent studies have integrated EDA and ML technologies to support this IR-drop-aware PDN design. In [1], authors used neural networks such as ANN/CNN or unsupervised learning such as clustering to estimate the IR-drop between each stage of the design flow.

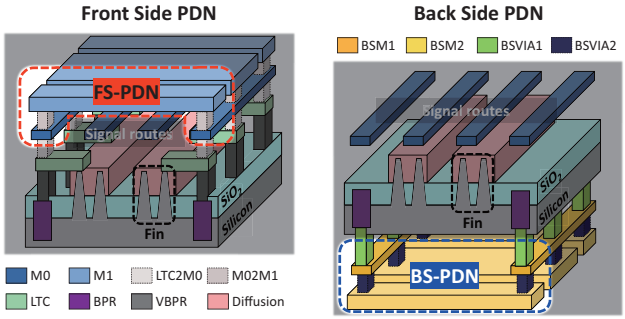


Fig. 1. (a): FS-PDN and (b): BS-PDN. Back-side (BS) technology provides dedicated back-side metal layers for power routing.

Meanwhile, back-side power delivery network (BSPDN) is now considered as a promising technology for addressing IR-drop issues. BSPDN refers to a power supply system in the backside of silicon composed of buried power rails, nanometer through-silicon vias (nTSV)s, and back-side metal. In conventional VLSI design that simultaneously designs signal and power on the front-side of silicon as shown in Fig. 1 (a), it is necessary to secure sufficient metal resources for power planning to reduce IR-drop. However, as technology nodes scale, the number of tracks in a standard cell decreases. This leads to a scarcity of available resources in terms of both power and signal [3]. Additionally, the width of Back-End-of-Line (BEOL) metal becomes much narrower, resulting in a corresponding rise in metal resistance [4]. On the other hand, Fig. 1 (b) shows the possibility of separating signal and power, and securing sufficient resources for PDN construction on silicon's backside [5]. Studies like [6] and [7] compared BSPDN's PPA (power, performance, and area) and thermal with FSPDN to demonstrate its potential.

In this paper, we propose an RL-based optimization for designing BSPDNs with minimal IR-drop. In our pathway, we

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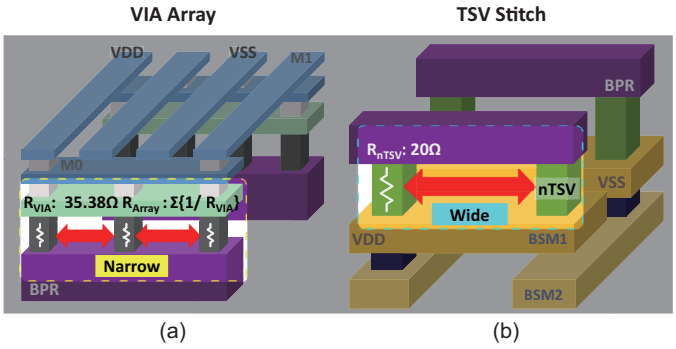


Fig. 2. (a): Via-array (FS-PDN) and (b): nTSV-stitch. nTSV requires a larger pitch than vias on the front-side metal. Thus, nTSV (20 Ω each) forms a larger resistance than FS vias that can form arrays in PDN design (35.4 Ω per each via, smaller in array)[1].

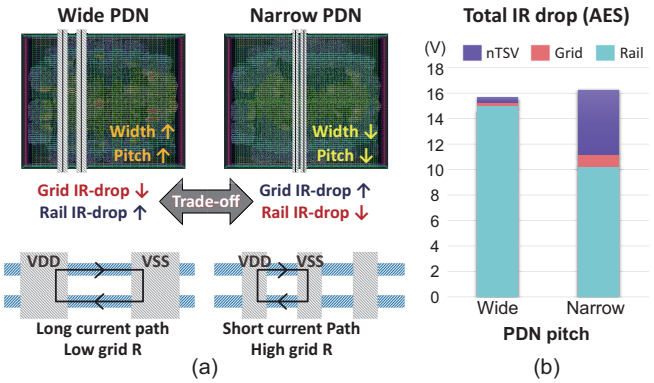


Fig. 3. (a) Wide PDN and Narrow PDN in back-side, and (b) IR-drop breakdown between Wide/Narrow PDN. Note the different contributors to IR-drop between Wide/Narrow in BSPDN[2].

provide a methodology to design VLSI that consists BSPDNs. Previous studies on BSPDN either concentrated on (1) the back-side (BS) processes, (2) circuit designs to enhance PDN performance, or (3) just presented results on PPA and thermal analyses compared to the front-side PDN. However, this study presents an actual methodology and results on how to design and optimize BSPDN at the VLSI level.

BS technology has a unique design environment. First, BSPDN uses nTSVs that have different resistance and pitch compared to conventional vias (discussed in Sec. II). Also, it has no signal routing, which is highly different from FSPDN [6]. Due to this unique environment, BSPDN optimization is different from previous FSPDN optimization and requires a different approach to solve. Finally, existing ML-based front-side PDN optimization studies use supervised or unsupervised learning, which is highly dependent on the training dataset, and most of them only focus on predicting IR-drop. However, our proposed methodology uses reinforcement learning while allowing the agent to interact with the environment and to find an optimized power grid pattern by itself without huge training dataset. We highlight our contributions as follows:

- We propose an RL-based BSPDN optimization framework to design an optimal power grid that minimizes IR-drop.
- To the best of our knowledge, we are the first to present a design flow for considering BS technology into place and route (P&R) and the PDN design process with commercial EDA tools.
- We used RL to efficiently solve the optimization problem without a large amount of training dataset and proposed novel ML-based optimization methodology which is different from previous FSPDN research that concentrated only on IR-drop estimation.
- The proposed framework successfully derived an optimized set of power grid widths for each different benchmarks and achieved a total IR-drop improvement with a maximum enhancement of up to $-19.0\%$ in static analysis and up to $-18.8\%$ in dynamic analysis.

[1]Note the considerable resistance of the nTSV compared to the via array. Due to this large resistance, the IR-drop contribution of the nTSV is higher in the Narrow PDN, as shown in Fig. 3.

## II. Background & Motivation

### A. Unique Design Environment in Back-side PDN

Back-side technology has some uniqueness in the PDN design. Fig. 2 (a) illustrates the traditional PDN design (front side) preferring via arrays for power mesh construction. Due to high-level parallelism, arrayed vias reduce their resistance and IR-drop. This flexible PDN design is also possible because conventional FS vias have a small pitch. However, BSPDN is different from FSPDN in the following reasons: First, as shown on the Fig. 2 (b), nTSV pitch is significantly higher than traditional via array. Therefore, designers have a highly limited amount of freedom when designing a PDN mesh. Second, nTSVs have a lower resistance (20Ω) than traditional vias (35.4Ω, [8]). Nevertheless, given its inability to be formed in an array or sparse mesh stripe, nTSV is a more significant contributor to the IR-drop in PDN.

### B. Grid/Rail/nTSV IR-drop trade-off in BSPDN

Understanding the unique design environment of the BSPDN, let us report the IR-drop trade-off between power rails and grids with nTSVs in BSPDN. In this experiment, we design two power grids (wide and narrow) and report the IR-drop in each PDN. As stated in Footnote 1([1]) and Fig. 3, the reported IR-drop (V) is the sum of the total IR-drop in each PDN node. The results in Fig. 3 provide the following insights. In general, power grids are designed as alternating VDD and VSS [9]. Naturally, the resistance of the grid decreases as the grid width increases, and the grid IR-drop decreases subsequently. However, as shown in Fig. 3 (a), the path of the current passing through the rail becomes longer on average as the pitch between VDD and VSS widens, resulting in an increase in the IR-drop of the rail. On the contrary, as

[2]Discussed in Sec. IV, Total IR-drop is the sum of the IR-drop seen by all metals and nodes. As discussed in Fig. 2, note that the via resistance is a significant contributor to IR-drop in a Narrow PDN, due to the large TSV resistance.

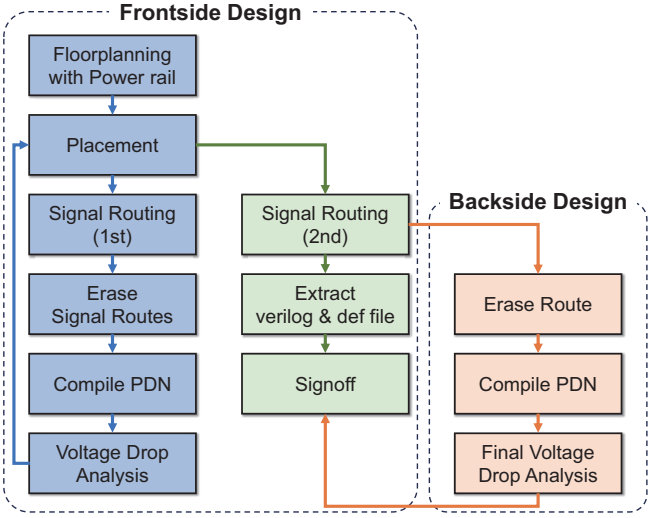


Fig. 4. Proposed place and route workflow with BSPDN. Our workflow allows design and optimization in the whole process of P&R with BSPDN.

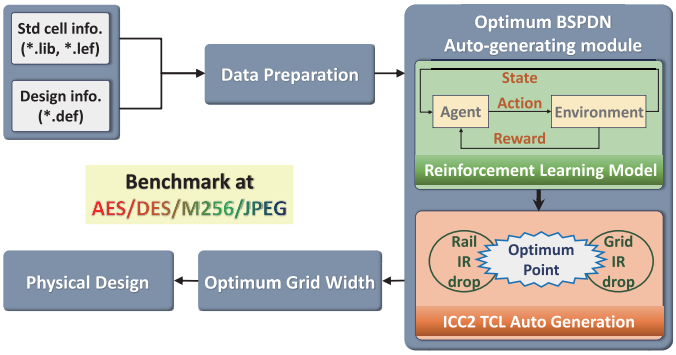


Fig. 5. Our PDN optimization framework using Reinforcement Learning.

shown in Fig. 3 (a), the resistance of the grid increases when the grid width decreases, but the pitch between the VDD and VSS becomes narrow. This leads to a shorter current path, on average, passing through the rail. Accordingly, the IR-drop of the rail decreases. This phenomenon is demonstrated in Fig. 3 (b), using commercial tools.

To address the trade-off limitation, it is feasible to enhance the overall IR-drop by implementing a grid with flexible width. Widening the grid width can be a design strategy if the grid IR-drop occurs relatively higher than rail's. If the opposite is the case, the grid width can be reduced to mitigate the total IR-drop. This idea allows for an optimal power grid width set that reduces the trade-off point IR-drop. Therefore, in PDN design, we can minimize IR-drop by using an abundant metal resource on the back-side.

## III. Proposed Methodology

This section proposes our BSPDN optimization methodology utilizing reinforcement learning (RL). First, we propose the physical design workflow for BSPDN designs. We mainly use *IC Compiler II* (ICC2) for placement and routing (P&R),

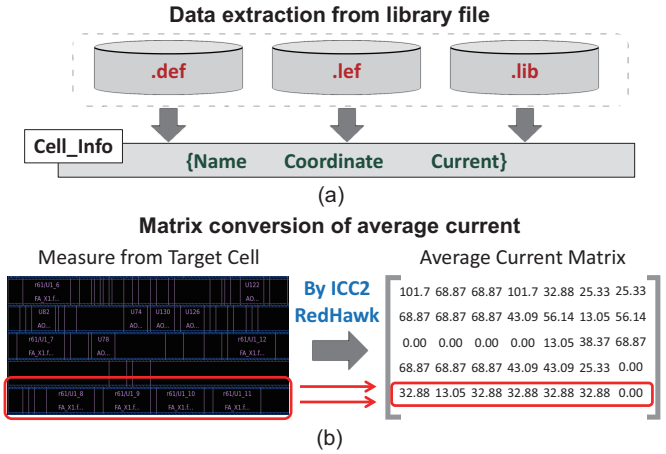


Fig. 6. (a) Required data (cell name, coordinate, current) from the technology files of the full-chip design, and (b) An example of how a Current Matrix (raw input data for RL) is extracted from the actual design in IC Compiler II.

and *Ansys RedHawk* for IR-drop analysis in this process. Following this, we provide an overview and the details of our propsed design framework.

### A. Physical Design Flow of BSPDN

We propose a design flow as shown in Fig. 4 to effectively design and analyze BSPDN using commercial tools. With synthesized netlist, we employ ICC2 to perform a first-order P&R phase, excluding the PDN design. Conventional P&R tools typically process IR-drop-aware design from placement to post-route optimization. Thus, we temporarily remove routing, design the back-side PDN, and reflect the IR-drop results analyzed by *RedHawk* in the placement phase again. Then, we proceed with secondary signal routing and finalize the front-side design. In addition, a back-side design block is also generated by eliminating the routing on the front-side and creating PDN, which accurately represents the conditions on the back-side. Using this method, we can perform the entire process of P&R considering the characteristics of BSPDN.

In our approach to back-side PDN design, we use a tech-file that includes back-side metal characteristics and design rules. Additionally, with identical cell placement of front and back-side, the front-side routing is preserved virtually on the back-side design block although it is physically eliminated. Consequently, signal and power can be designed separately into two blocks, which represent the designs of the front-side and back-side. In this study, we only utilize back-side design methodology in our flow to implement the optimal PDN from the proposed design framework.

### B. Overview of Design Optimization Framework

Based on our physical design methodology, Fig. 5 shows the overall flow of our proposed BSPDN design optimization framework. First, we gather and process the essential design information that the RL model needs. Then, we identify the optimal back-side power grid configurations that minimize IR-drop by employing an RL model that effectively addresses the

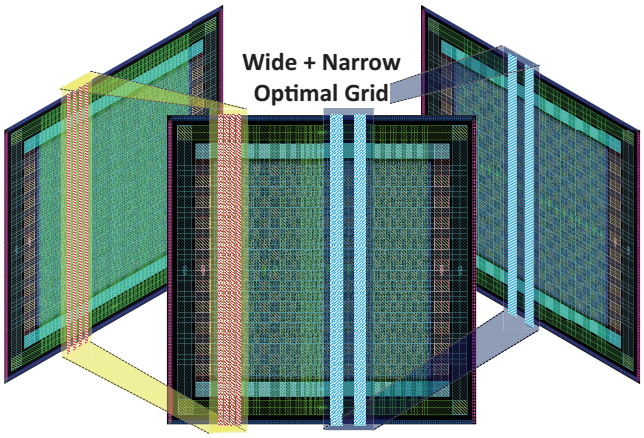


Fig. 7. Proposed PDN is the result of the optimal grid width set of the actual design from the reinforcement learning model.

BSPDN optimization challenge. Finally, we apply the derived grid set to the actual physical design.

### C. Reinforcement Learning Model

To determine the optimal power grid width that minimizes the IR-drop, we refine the input data and build an RL model specific to the BSPDN optimization problem. We used Python for the RL implementation.

*1) Data Preparation:* Before starting reinforcement learning, we must prepare the cells and available design information for our model. Fig. 6 shows this process. First, we use cell lef and liberty file (.lib) to determine the name and power consumption of the standard cell. Then, we extract the location of the cell inside the design from the def file. To facilitate the computation of the reinforcement learning model, we divided the core region into small blocks and represented the block current as a matrix. The length of one side of each block is set to the pitch of the narrow grid at the trade-off point. The reinforcement learning model can effectively predict the IR-drop and find the optimum point with this pre-calculated block current matrix.

*2) RL Environment:* The concepts of RL model with BSPDN optimization problem are as follows.

- State: States represent a specific set of grid widths. For example, a state of (4, 4, 1, 1) illustrates a (Wide, Wide, Narrow, Narrow) grid width pattern. Also, the improvement factor is determined inside the state by utilizing the block current matrix processed in Sec. III-C1. The method for calculating this improvement factor ($\alpha$) is as follows. We extract the median rail and grid IR-drop for each uniform wide and narrow grid at the tradeoff point. Next, we calculate the number of IR-drop lower than the median value extracted from the corresponding grid width pattern and divide by the number of rails or grids. We use the improvement factor to determine the reward.
- Action: Action is an index to determine the next state. For example, if you take (W, W, N, N) as an action in the state (1, 1, 4, 4), the state will transit to (4, 4, 1, 1).

TABLE I
DETAILS OF OUR BACK-SIDE PROCESS BASED ON [8] AND [3].

| Metal layer | Resistance [$\Omega/\mu m$] | Pitch [$nm$] | Reference |
|---|---|---|---|
| BPR | 20.330 | 0.36 | [4] |
| BSM1 | 1.833 | - | [3] |
| BSM2 | 1.374 | - | [3] |
| **Via layer** | **Resistance [$\Omega$/via]** | **Pitch [$\mu m$]** | **Reference** |
| BS via | 0.430 | - | [3] |
| nTSV | 20.000 | 0.10 | [3] |

TABLE II
SPECIFICATIONS OF THE PDN IN OUR BENCHMARKS [11]

| Bench mark | Area [$\mu m^2$] | Clock [$GHz$] | Grid width [$\mu m$] | |
|---|---|---|---|---|
| | | | Wide | Narrow |
| AES | 35.700 × 35.736 | 3.125 | 1.44 | 0.36 |
| DES | 70.950 × 70.848 | 4.350 | 2.88 | 0.72 |
| M256 | 127.350 × 127.296 | 0.200 | 5.76 | 1.44 |
| JPEG | 158.050 × 158.040 | 1.250 | 5.76 | 1.44 |

- Reward: Reward is an indicator of how close you are to the optimum grid width set. The expression to determine reward is Eq. (1). The rail and grid improvement factors computed by state will return the maximum reward as long as they are less than or equal to 0.5 and closer to zero. If either value is zero, it is treated as Eq. (2). On the other hand, there are cases where rail and grid IR-drop do not improve simultaneously with changes in grid width. In this case, the reinforcement learning model only finishes learning after the optimal point is found. Therefore, if the IR-drop of either rail or grid is below 0.5, we restrictively terminate learning and give a negative reward according to Eq. (1). We used the reward calculated from these mechanisms and equations to update the Q-value of the action taken in a particular state. The Q-value update equations can be found in [10].

$$Reward = \begin{cases} \frac{1}{\alpha_{\text{grid}} \cdot \alpha_{\text{rail}}} & \text{if } \alpha_{\text{grid, rail}} < 0.5 \\ -|\alpha_{\text{grid}} \cdot \alpha_{\text{rail}}| & \text{otherwise} \end{cases} \quad (1)$$

$$Reward = \begin{cases} \infty & \text{if } \alpha_{\text{grid, rail}} = 0 \\ \frac{1}{\alpha_{\text{grid}}^2} & \text{if } \alpha_{\text{rail}} = 0 \text{ and } \alpha_{\text{grid}} \neq 0 \\ \frac{1}{\alpha_{\text{rail}}^2} & \text{if } \alpha_{\text{grid}} = 0 \text{ and } \alpha_{\text{rail}} \neq 0 \end{cases} \quad (2)$$

### D. Design Implementation

To address the problem that RL learning time increases with design footprint, we partition the design where we apply RL. This lets us find the best grid width even for the large footprint. ICC2 implementation scripts are generated automatically using Python afterward. Figure Fig. 7 shows the result of an AES benchmark design.

## IV. EXPERIMENTAL RESULTS & DISCUSSIONS

In this section, we compare the IR-drop of our optimized-with-RL BSPDN with Narrow or Wide schemes to each benchmark. We perform block-level P&R and IR-drop measurements using *Synopsys IC Compiler II* and *RedHawk* in the 5nm FinFET standard cell library [4]. Furthermore, we present

TABLE III
IR-DROP RESULTS BY STATIC AND DYNAMIC IN EACH BENCHMARK. WE FIRST EXTRACT IR-DROP ON EVERY NODE/METAL, THEN SUM ALL THE IR-DROP NUMBERS BASED ON EACH CATEGORY. THE TOTAL IR-DROP IS THE SUM OF RAIL, GRID, AND VIA IR-DROP.

| Bench mark | Simulation type | Grid | Rail IR-drop [V] | Grid IR-drop [V] | Via IR-drop [V] | Total IR-drop [V] | Compared ratio [%] |
|---|---|---|---|---|---|---|---|
| **AES** | **Static** | Wide | 15.00 | 0.25 | 0.40 | 15.64 | 114.94 |
| | | Narrow | 10.32 | 1.00 | 5.10 | 16.42 | 118.98 |
| | | Optimized | 11.36 | 0.50 | 1.44 | 13.30 | 100.00 |
| | **Dynamic** | Wide | 15.02 | 0.25 | 0.40 | 15.67 | 115.80 |
| | | Narrow | 10.20 | 0.99 | 5.04 | 16.24 | 118.76 |
| | | Optimized | 11.26 | 0.49 | 1.44 | 13.19 | 100.00 |
| **DES** | **Static** | Wide | 208.81 | 2.65 | 3.39 | 214.85 | 108.61 |
| | | Narrow | 159.36 | 9.99 | 47.33 | 216.67 | 109.38 |
| | | Optimized | 168.86 | 6.12 | 21.38 | 196.36 | 100.00 |
| | **Dynamic** | Wide | 225.07 | 2.83 | 3.62 | 231.52 | 109.03 |
| | | Narrow | 170.63 | 10.65 | 50.47 | 231.74 | 109.12 |
| | | Optimized | 181.23 | 6.53 | 22.85 | 210.61 | 100.00 |
| **M256** | **Static** | Wide | 85.89 | 0.55 | 1.50 | 87.93 | 109.26 |
| | | Narrow | 62.05 | 2.35 | 23.20 | 87.60 | 108.91 |
| | | Optimized | 71.07 | 1.03 | 7.69 | 79.79 | 100.00 |
| | **Dynamic** | Wide | 73.46 | 0.55 | 0.69 | 74.70 | 108.10 |
| | | Narrow | 58.58 | 2.36 | 11.57 | 72.51 | 105.34 |
| | | Optimized | 62.79 | 1.58 | 4.28 | 68.65 | 100.00 |
| **JPEG** | **Static** | Wide | 1195.51 | 7.63 | 10.32 | 1213.46 | 111.36 |
| | | Narrow | 935.63 | 33.79 | 168.25 | 1137.67 | 105.46 |
| | | Optimized | 1003.79 | 18.73 | 53.08 | 1075.61 | 100.00 |
| | **Dynamic** | Wide | 1274.07 | 8.12 | 10.99 | 1293.17 | 111.62 |
| | | Narrow | 992.85 | 35.95 | 178.98 | 1207.77 | 105.37 |
| | | Optimized | 1066.34 | 19.97 | 56.59 | 1142.90 | 100.00 |

the efficiency of RL-based methodology through design time compared to conventional manual optimization.

### *A. Design Specification*

Table I shows the key values and dimensions of back-side process components. The resistance and pitch of the metal layer (BPR, BSM) and via layer (BS via and nTSV) are based on [3] and [8]. The power mesh consists of two layers. We apply the optimum grid width to the upper layer (BSM1) since PDN optimization is applied between BPR and BSM1, which nTSV connects. Therefore, in the lower layer (BSM2), we design a PDN with a uniform grid width (see Fig. 1 for details of the layer configurations). We implement the block-level design by using the benchmarks of OpenCores [11]. Table II presents the design specification of each benchmark for IR-drop analysis. Each benchmark has different wide and narrow grid widths to minimize the IR-drop of the grid and rail, respectively. Note that, as mentioned in Sec. II-A, all grid widths are designed to be multiple of integer 180 nm, which is the pitch of the nTSV.

### *B. Total IR-drop Result & Further Exploration*

Table III shows the static and dynamic IR-drop analysis results of the optimized PDN for each benchmark. Note that the total IR-drop is the sum of rail and grid IR-drop. The optimized PDN has an average static IR-drop of $-8.69\%$ than the wide or narrow scheme. We also present dynamic IR-drop results based on vectorless analysis with an activation rate of $5\%$. As a result, the optimized PDN shows an IR-drop improvement of $-8.31\%$ compared to the uniform PDN in dynamic analysis. The optimized PDN through the RL model has better quality than the uniform PDN to achieve effective IR-drop reduction.

Fig. 8 shows a visual IR-drop map of the AES benchmark, demonstrating the reduction of max IR-drop with optimized PDN. As shown in Fig.8 (a), the optimized PDN has a smaller grid IR-drop than the narrow PDN. Similarly, In Fig. 8 (b), optimized PDN has fewer IR-drop red zones than wide PDN. Among the four benchmarks, the smallest one, AES, shows the greatest $-18.76\%$ IR-drop improvement over the uniform. The main reason is that a benchmark with a small footprint has less conflicts between actions that either increase or decrease width during optimization compared to the larger benchmarks. This raises the possibility that optimizing large blocks by splitting them into smaller blocks may achieve further IR-drop improvement.

### *C. Comparison of Design Optimization Time*

We present the time impact of the optimal PDN design with the RL model in Fig. 9. In average, the training time using our model takes 250.5 minutes. Though this may seem long, this is a small amount of time compared to manual optimization. Manual optimization has to analyze the IR-drop of all possible grid width cases. Therefore, we calculated the total time of manual optimization by multiplying the runtime of a single *RedHawk* analysis and the number of possible cases. RL optimization reduces the runtime by $-89.6\%$ on average compared to manual. For example, in the DES case, the runtime of RL optimization is $-96.9\%$ less than manual. M256 requires $3.94\times$ larger runtime than the AES, but this is

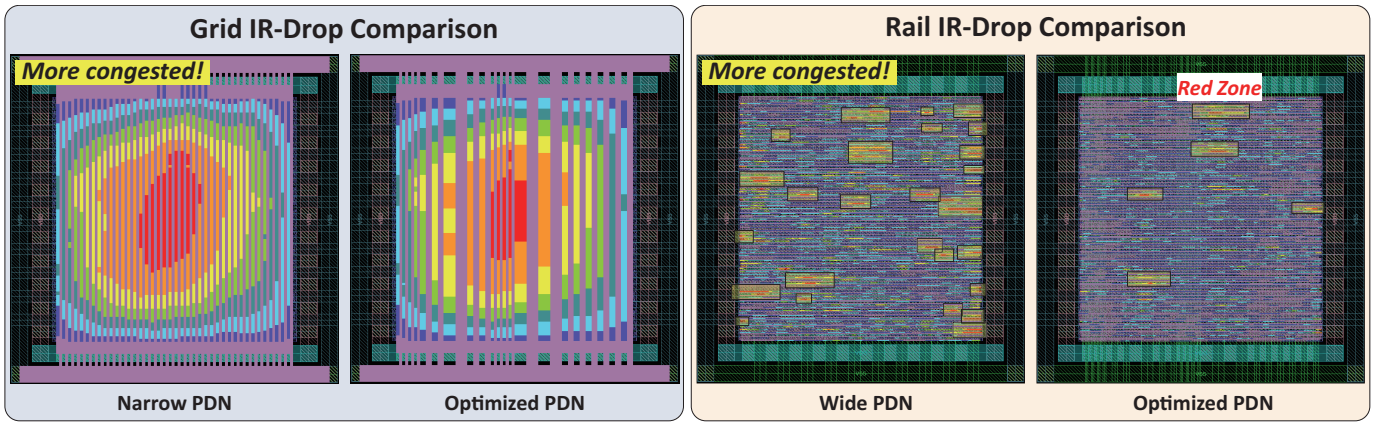


Fig. 8. IR drop results in AES benchmark. (a): Grid (mesh) IR-drop results between narrow and optimal. (b): Rail IR-drop results between wide and optimal. Our optimized PDN reports less red zones (high IR-drop) in both (a) and (b).

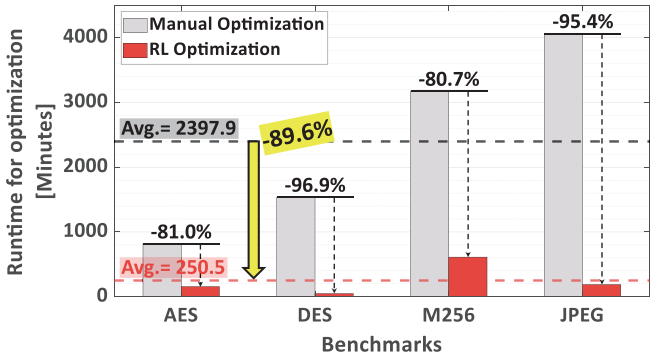


Fig. 9. Runtime comparison between RL and manual optimization. The RL reduces an average design time about $-89.6\%$ compared to the manual.

still significantly small compared to the manual runtime. Thus, we note our framework could highly contribute to reducing the optimization runtime compared to manual optimization.

## V. Conclusion and Future Work

In this study, we propose a novel RL-based design optimization framework for BSPDN in VLSI design. We develop a design flow and process assumptions for BSPDN and establish an RL model to efficiently solve the BSPDN optimization problem. As a result, the proposed design framework finds the design-specific optimum grid width set and applies it to the actual physical design. Our proposed framework shows an average IR drop improvement of $-8.69\%$ and a maximum of $-19.0\%$ in static analysis. It also shows an average reduction of $-8.31\%$ and a maximum of $-18.8\%$ in dynamic IR-drop analysis. In addition, from the perspective of design time, our RL model solves the optimization problem more efficiently, compared to manual optimization.

We present a methodology that can effectively meet the IR-drop constraint by utilizing the design flexibility of BSPDN. However, there is still room to design PDN in various forms by utilizing abundant metal resources. Therefore, our future work is to study the most optimal form of PDN that reduces IR-drop even as the size of the design increases in various forms. Last but not least, we present our contribution of full-automation in completing back-side power planning without human intervention.

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