Testing Algorithms for Hard to Detect Thermal Crosstalk Induced Write Disturb Faults in Phase Change Memories

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***Abstract* – Phase change memory (PCM) is a promising non-volatile memory technology, to serve as storage class memory in modern systems. However, during write operations on PCM cells, high temperatures are locally generated for the heating of the used phase change material. The heat diffusion may influence adjacent cells (thermal crosstalk), leading to the generation of write disturb faults and the appearance of errors in the data stored in the memory array. Moreover, as technology scaling increases proximity among cells, the probability of thermal crosstalk influence is also increased. Thermal crosstalk is a key reliability challenge in PCMs. Although various techniques have been proposed to alleviate its influence, it may affect the memory operation under special conditions that maximize the heat in the neighborhood of a cell. Due to these special conditions, the corresponding write disturb faults are hard to detect. Existing testing solutions in literature are not capable of producing such conditions and may fail to cover those hard to detect faults. In this paper, we propose effective testing algorithms, capable of generating proper conditions for the activation and detection of hard to detect thermal induced write disturb faults, at a cost-efficient manner. The algorithms' complexity varies from 3MxN to 10MxN (where M and N are the number of memory array rows and columns respectively).**

Index Terms – Phase Change Memory (PCM), Thermal Crosstalk, Write Disturb Faults, Hard to Detect Faults, Testing Algorithms.

I. Introduction

Phase Change Memory (PCM) is a non-volatile, high density, memory suitable to be used as a storage class memory (SCM). It offers faster access times than NAND Flash memory and lower cost as well as longer data retention time than the dynamic random-access memory (DRAM) [1]. In addition, PCM showed to have a scalability and access latency comparative to DRAM and a write endurance stronger than Flash, while the write energy is scaling down with feature size so that it decreases with dimension [2], [3], [4]. Moreover, PCM and DRAM have the same hierarchical organization.

However, PCM still faces several challenges towards its widespread adoption as a "universal" memory. Among them, research efforts show that PCM technology scaling endangers the memory reliability [5]. The main reason stems from technology scaling in the nanometer era, which increases the proximity of the cells, leading to the appearance of disturbance failures due to the heat generation and diffusion among adjacent cells (thermal crosstalk) during write operations [3], [6], [7], as we will analyse in next section. Thus, in the presence of thermal crosstalk, a write disturb fault may arise, which is an unwanted logic data change in a neighbouring cell (victim cell). Although, various techniques are considered for the mitigation of thermal crosstalk and the effective reduction of write disturb faults, the problem still remains in case of vulnerable cells under special heating conditions (these are hard to detect faults). Existing testing algorithms are not capable to generate the required heating conditions, which in turn may result to fault escapes during manufacturing testing.

In this work, we present new testing algorithms for hard to detect thermal crosstalk induced write disturb faults in PCMs at nanometer technologies. These algorithms maximize the heat in the neighborhood of a cell, by sequentially performing proper write operations to its adjacent cells, aiming to activate the write disturb mechanism under worst case conditions.

The paper is organized as follows. In Section II, the PCM concept is discussed, and the thermal crosstalk phenomenon is analyzed. In addition, existing thermal crosstalk related write disturb fault testing algorithms for PCMs are quoted. Next, in Section III, we present the proposed testing algorithms that are capable of activating and detecting PCM thermal crosstalk induced write disturb faults, under excess heat conditions in the neighborhood of each cell in the memory array. Section IV provides comparisons among the above write disturb oriented testing algorithms, with respect to their complexity and their ability to cover hard to detect faults. Finally, the conclusions are drawn in Section V.

II. Preliminaries

A. The Phase Change Memory Concept

Phase Change Memory stores data using two states of a phase change material, usually $Ge_2Sb_2Te_5$ (GST) chalcogenide: high resistance amorphous RESET state (logic '0') and low resistance crystalline SET state (logic '1'). It consists of the top metal electrode, the GST, the heater and the bottom electrode [8]. A PCM cell is programmed (written) by injecting electrical pulses to heat GST and change the resistance state [9], [10]. The PCM cell is programmed to the high resistance RESET state (a zero logic state is stored) when

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a short duration, but large amplitude, current pulse is applied (see Fig. 1), so that the GST is heated (through Joule heating effect) above its melting temperature (T_{melt}>600°C) and then quickly cooled down. RESET programming consumes the largest power since the cell needs to reach the melting temperature. RESET current is determined by various material properties such as the resistivity and thermal conductivity as well as the device structure. When a long duration but small amplitude current pulse is injected, the PCM cell is programmed to the low resistance crystalline SET state (an one logic state is stored). In a SET operation, the inner-cell temperature goes above GST crystallization point (T_{crys}=100°C ~ 150°C), but below GST melting point. In general, the operating speed of PCM is limited by the SET programming time because it takes finite time to fully crystallize the amorphous region. To read the cell state, its resistance is measured by applying a current pulse, small enough not to disturb the existing state.

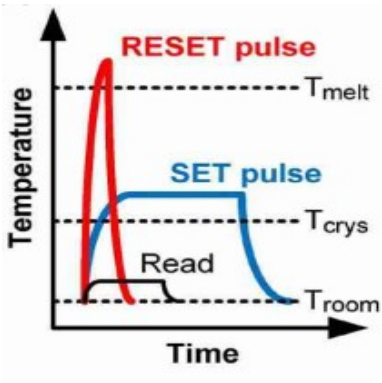

Fig. 1. PCM cells are programmed and read by applying electrical pulses which change temperature accordingly.

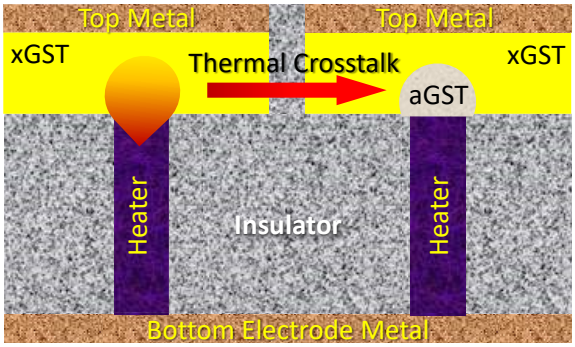

Fig. 2. The thermal crosstalk mechanism.

B. Thermal Crosstalk in PCMs

PCM cells are programmed using current pulses to heat the phase change material and alter its resistance between a low resistance crystalline state (SET) and a high resistance amorphous state (RESET). The crystalline state is stable while the amorphous state is thermodynamically unstable. Thus, when the amorphous material is heated, it easily changes into the crystalline state [11]. During the RESET operation on a cell (aggressor), where intense programming currents are used, high temperatures at the GST area of the cell are generated [12] (the heat produced during a RESET operation is more than two times the heat produced during a SET operation [13]). The resultant heat diffusion may disturb neighbouring idle cells (victims) that are in the thermodynamically unstable amorphous (RESET) state and turn them to the crystalline (SET) state (see Fig. 2) [7], [14]. This is the thermal crosstalk phenomenon [15], which is modelled as a write disturb (WD) fault (Fig. 3). The strength of thermal crosstalk is related to improper isolation issues or existing defects (e.g. a weak cell) [16]. By the activation of a WD fault, errors are generated in the data stored in the memory. As technology scaling considerably increases proximity among cells and reduces the size of cells, this heat influences the state of neighbouring cells with increasingly high probability [3], [6], [17], either in the wordline (WL) or the bitline (BL) direction.

The strength of thermal crosstalk influence depends on many factors like the cell structure, the inter-cell distance, the RESET pulse width, or the thermal conductivity of the interlayer dielectric [7]. Various techniques have been investigated with the aim of reducing thermal crosstalk effects. Among them are the replacement of the commonly used mushroom cell structure with the confined cell structure [4], the use of a carbon-based liner in the cell structure that works as a heat insulator [1], the introduction of thermal barriers around the phase change material [18], [19], the use of pattern-based data compression techniques [13], the use of encoding techniques [20] or the combined use of compression and encoding techniques [3] to reduce the thermal crosstalk related error rate (at the cost of silicon area redundancy). However, all the above solutions may alleviate but not eliminate the thermal crosstalk influence. Consequently, it is mandatory to develop appropriate testing methodologies and algorithms for the detection of thermal crosstalk induced write disturb faults, aiming to ensure PCM devices of enhanced reliability.

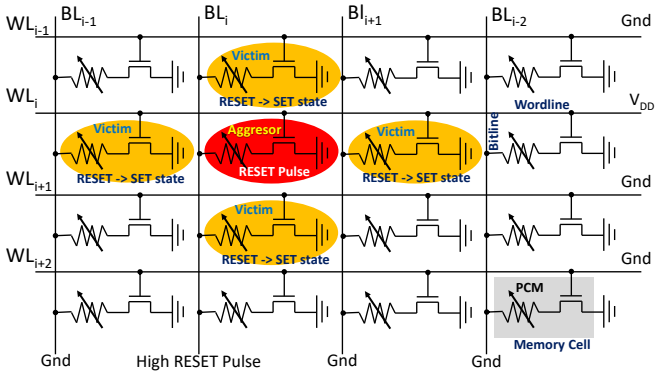

Fig. 3. Memory organization and the thermal crosstalk write disturb effect.

C. Thermal Crosstalk induced WD Fault Testing Solutions

Towards the detection of thermal crosstalk induced write disturb faults (TC-WDF), few March based testing algorithms have been proposed in the open literature. In [21], the March-PC algorithm is proposed that covers TC-WDFs with a complexity of 11MxN operations (where M and N are the number of rows and columns in the memory array respectively), which is improved in [22] (with the March-

PCM algorithm) by reducing the complexity down to 8MxN operations. Due to the linear addressing scheme of these algorithms, it is not feasible to efficiently excite TC-WDFs by performing RESET operations to all four in close proximity (adjacent) neighbouring cells (aggressors) to a victim cell, aiming to disturb the latter. For that reason, in [23] the snake addressing scheme is adopted to effectively excite TC-WDFs. Through snake addressing, all four adjacent cells to a victim cell perform a RESET operation, activating this way the disturb accumulation phenomenon. According to this phenomenon, consecutive RESET operations on cells adjacent to the victim cell eventually accumulate the stress to gradually change the victim to the crystalline state. The corresponding March-PDF testing algorithm has a complexity of 3MxN.

However, due to the snake addressing scheme, the March-PDF algorithm although it achieves to perform the RESET operation on all four adjacent cells to the victim cell, these operations are not sequential, having a time distance among them, which increases with the memory array size. Since technology evolution offers various techniques to reduce thermal crosstalk effects in a PCM memory (see previous subsection [1], [4], [7], [18]), this time distance among the RESET operations may not activate the TC-WDF generation mechanism (hard to detect faults), as the heating of the victim cell will be restricted. Thus, all the above testing algorithms are not suitable to cover those hard to detect TC-WDFs. An ideal strategy for the activation and detection of these faults would be to perform sequential RESET operations on the adjacent cells (the one after the other) of every cell in the memory array. This way, the maximum heat is developed in the neighbourhood of the victim cell due to the almost concurrent activation of all four aggressor cells, enabling the sensitization and detection of the hard to detect TC-WDFs under consideration. Appropriate testing algorithms for the above faults are proposed in the next section.

III. Testing Algorithms for Hard to Detect Thermal Crosstalk Induced Write Disturb Faults

Two new testing algorithms, aiming to cover hard to detect TC-WDFs, are presented next. In the development of these algorithms, we will use the notation adopted for the Neighborhood Pattern Sensitive Fault (NPSF) model. Specifically, we will exploit the Type-1 neighborhood [24].

A. Sequential Activation of Four Adjacent Cells

For the first algorithm, we will exploit the typical Type-1 tiling neighborhood [16], [24], as shown in Fig. 4, which is suitable for the required operations, described in Section II, on the four adjacent cells to a victim cell. According to the Type-1 tiling neighborhood, the memory array is totally covered by a group of neighborhoods which do not overlap. Each neighborhood consists of the four adjacent cells to a base cell, these on the same row and the same column, which form the deleted neighborhood. Thus, this is a five cells neighborhood and the cells in each neighborhood are numbered from 0 to 4. In the example of Fig. 4, cell 2 is the base cell and cells 0, 1, 3 and 4 form the deleted neighborhood. Equivalently, every other type of cell (0 or 1 or 3 or 4) can be considered as base cell. In what follows, in a neighborhood, the cells of the deleted neighborhood will play the role of aggressors while the base cells will be the victims.

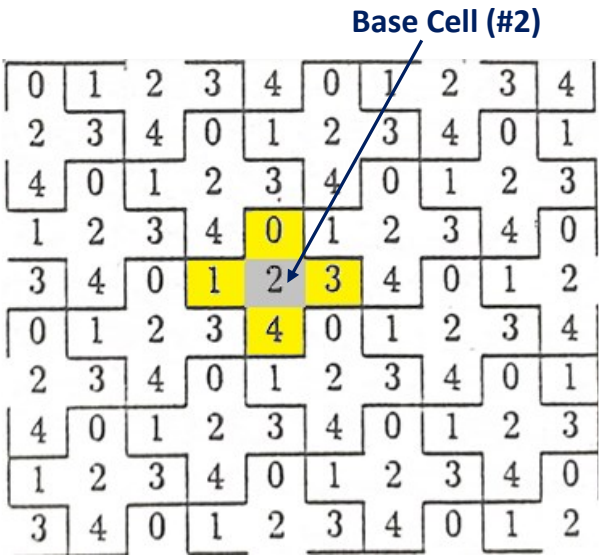

Fig. 4. Typical Type-1 tiling neighborhoods

The testing algorithm consists of five sessions (one session for each base cell type (0, 1, 2, 3 or 4)) and each session is composed of three steps, as follows:

Session A – Base Cell is cell #0

Step 1. Perform write operations by programming all base cells to the RESET state (logic 0) and all cells in the deleted neighborhoods to the SET state (logic 1). This is a total of MxN operations.

Step 2. Perform write operations by sequentially programming the cells of each deleted neighborhood to the RESET state. The cells of the deleted neighborhoods make transitions from logic 1 to 0. This is a total of (4/5)MxN operations.

Step 3. Read the base cells in each neighborhood. The expected logic value is 0. This is a total of (1/5)MxN operations.

The total number of operations in Session-A is 2MxN.

Next, there are four more Sessions B, C, D and E, with exactly the same three steps, where cells 1, 2, 3 and 4 are set as base cells respectively. Thus, the application of the whole test procedure requires a total of 10MxN operations (which is also the algorithm complexity). After its completion, all cells in the memory array have been tested for hard to detect TC-WDFs, since all cells in their deleted neighborhood sequentially performed the RESET operation.

For example, in Session-C, where cells #2 are the base cells, a possible progress of the test procedure in Step 2 (a possible addressing mode among other equivalent alternatives) is illustrated in Fig. 5. "*Thunderbolt*" like paths are formed.

Dashed (red) lines do not imply any programming operations. Obviously, cells #2 are not written in the second step of this session. Given that the base cell is cell $C_{i,j}$ (where i is its row number and j is its column number), the RESET operations will be sequentially performed on the cells of the deleted neighborhood in the following order:

$$C_{i-1,j} \rightarrow C_{i,j+1} \rightarrow C_{i,j-1} \rightarrow C_{i+1,j}$$

In practice, the number of write operations in Step 2 is less than (4/5)MxN (by 2/5(M+N) operations), since the cells #4 and #0 in the first and last row respectively, as well as the cells #3 and #1 in the first and last column respectively, are not written.

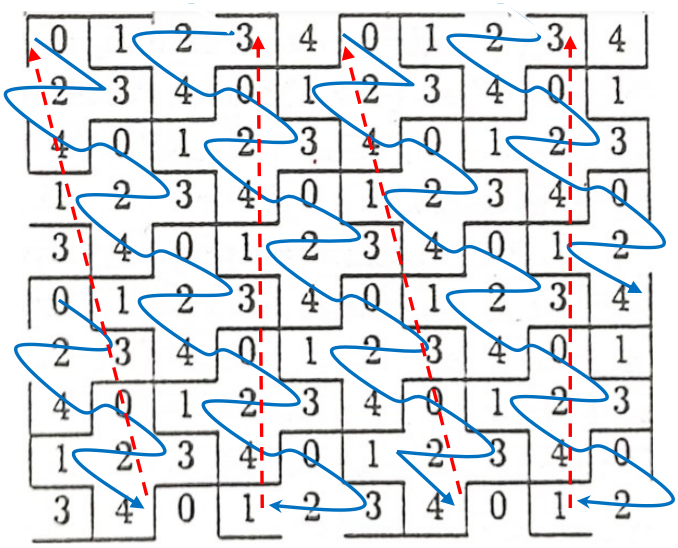

Fig. 5. Addressing mode of the "thunderbolt" algorithm.

By adopting the strategy proposed in [23], where for the detection of thermal crosstalk faults all cells in the memory are initially written to 0 (RESET state) and then RESET operations are performed on them, the total number of required operations can be reduced to 6MxN. In that case, Step 1 in Session-A is modified in order just to RESET all cells in the memory array, while this step is eliminated in the rest Sessions (B, C, D and E). All the other steps remain the same, so that a "*fast*" version of the "*thunderbolt*" algorithm arises. However, the strategy followed in [23] may not be quite effective for the testing procedures under consideration since the aggressor cells are already in the RESET state when RESET operations are performed on them.

B. Sequential Activation of Three Adjacent Cells

Obviously, the testing cost (in test time) is a crucial parameter in manufacturing testing. This cost is related to the number of operations that are required to apply a test procedure. On the other hand, depending on the technology used for the fabrication of a phase change memory, performing sequentially the RESET operation on only three from the four cells in the deleted neighborhood of a cell may be a capable condition for the activation of hard to detect TC-WDFs. Thus, the number of test operations can be reduced, reducing this way the test cost.

For the development of the new low-cost testing algorithm, we will exploit the two-group tiling method for the Type-1 neighborhood. The two-group method is based on the duality of the cells in Type-1 neighborhoods (a cell is either a base cell or a deleted neighborhood cell). Using this method, the cells are divided into two groups by a checkerboard pattern as shown in Fig. 6. A cell is a base cell (b) in one group and a deleted neighborhood cell (A, B, C or D) in the other group, and vice versa. The two-group tiling method can be also exploited for the development of the previous algorithm (e.g. for the sequential activation of four adjacent cells), however the complexity of the algorithm remains the same, while its analysis and description are quite more complicated.

The testing algorithm consists of two sessions (one session for each group) and each session is composed of three steps, as follows:

Session A – Left Group

Step 1. Program all base cells to the RESET state (logic 0) and all cells in the deleted neighborhoods to the SET state (logic 1). This is a total of MxN operations.

Sep 2. Perform write operations by sequentially programming to the RESET state the deleted neighborhood cells (A, B, C, D) of each base cell (b) in pairs of rows (1st and 2nd, 3rd and 4th, 5th and 6th and so on). The cells of the deleted neighborhoods make transitions from logic 1 to 0. This is a total of (1/2)MxN operations.

Step 3. Read the base cells (b) in the array. The expected logic value is 0. This is a total of (1/2)MxN operations.

The total number of operations in Session-A is 2MxN.

Next, follows Session B, with exactly the same two steps on the Right Group. Thus, the application of the whole test procedure requires a total of 4MxN operations. After its completion, all cells in the memory array, except the cells of the first and last columns, have been tested for hard to detect TC-WDFs, since at least three cells in their deleted neighborhood sequentially performed the RESET operation.

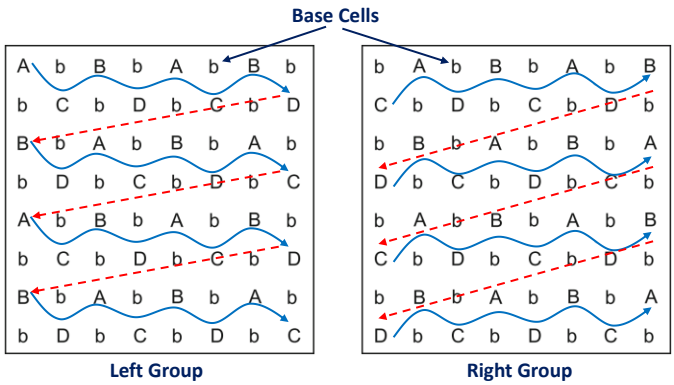

Fig. 6. The two-groups method and the addressing mode for the "wave" algorithm.

For example, in Step 2 of Session-A a possible addressing mode among other equivalent alternatives is illustrated in Fig. 6. "*Wave*" like paths are formed. Again, dashed (red) lines do not imply any programming operations. Obviously, base cells are not written in this step. Thus, in an odd row, for each base cell the three deleted neighborhood cells in the same row and the next row are sequentially written, while in an even row, the three deleted neighborhood cells of a base cell in the same row and the previous row are sequentially written. So, given that the base cell is cell $C_{i,j}$ and i is odd, the RESET operations will be sequentially performed on the cells of the deleted neighborhood in the following order:

$$C_{i,j-1} \rightarrow C_{i+1,j} \rightarrow C_{i,j+1}$$

Next, given that the base cell is cell $C_{i,j}$ and i is even, the RESET operations will be sequentially performed on the cells of the deleted neighborhood in the following order:

$$C_{i,j-1} \rightarrow C_{i-1,j} \rightarrow C_{i,j+1}$$

Once again, by adopting the strategy proposed in [23], where for the detection of thermal crosstalk faults all cells in the memory are initially written to 0 (RESET state) and then RESET operations are performed on them, the number of required operations can be reduced to 3MxN. In that case, Step 1 in Session-A is modified and all cells in the memory array are written to 0, while this step is eliminated in Session B. Steps 2 and 3 remain the same. This is the "*fast*" version of the "*wave*" algorithm.

For the base cells in the first and last column of the array in each group, few extra operations are required to apply the test correctly. Initially, in every group the base cells of the first and last columns are written to 0 (these are 2M operations in both groups), while the deleted neighborhood cells (A, B, C and D) of the first, second, penultimate and ultimate columns are written to 1 (these are another 4M operations in both groups). Then, the deleted neighborhood cells of the first, second, penultimate and ultimate columns are written to 0 (4M operations in both groups) and finally the base cells of the first and last columns are read, with expected value 0 (2M operations in both groups). This extra Session requires in total 8M operations, which is a very small additional cost to the cost of the main algorithm.

IV. Discussion and Comparisons

As mentioned in Section II.B, thermal crosstalk is a challenge for the development of phase change memories. Its presence may lead to write disturb faults that induce errors in the data stored in the memory array. Although, with technology evolution, various approaches for the alleviation of thermal crosstalk influence have been proposed and many of them adopted by the industry, the problem remains. For that reason, few testing methods (algorithms) have been presented in the open literature for the detection of thermal crosstalk induced write disturb faults – TC-WDFs [21], [22], [23]. In [21] and [22] the used March algorithms (March-PC and March-PCM) are not capable to efficiently excite hard to detect TC-WDFs by performing the required sequential RESET operations to all four or even at least three or two adjacent neighbouring cells to a cell before a programming operation on this cell. Moreover, the March-PDF testing algorithm [23] (which uses the checkerboard background patterns for the memory array initialization and a "snake" addressing scheme with diagonal programming operations for TC-WDF sensitization) although performs RESET operations on all four adjacent cells to a cell in the memory array, these operations are not sequential in order so that there is an increased probability not to be able to activate hard to detect TC-WDFs. In Table 1, comparisons are provided among TC-WDF related testing algorithms in the open literature and these proposed in our work. As the number of adjacent cells that are sequentially activated increases (see columns 3-5 in table), the capability of the testing algorithm to cover hard to detect TC-WDFs is strongly enhanced. Thus, although three of the four testing algorithms proposed in this work have a higher (but acceptable) complexity than the algorithm in [23], they provide the ability to effectively cover hard to detect TC-WDFs.

TABLE 1. Testing algorithms' Comparisons with respect to the complexity and their ability to cover hard to detect TC-WDFs.

		# of adjacent cells sequentially activated for the coverage of hard to detect TC-WDFs		
Algorithm	**Complexity**	**2 cells**	**3 cells**	**4 cells**
March-PC [21]	11MxN	–	–	–
March-PCM [22]	8MxN	–	–	–
March-PDF [23]	3MxN	✓	–	–
Thunderbolt	10MxN	✓	✓	✓
Fast Thunderbolt	6MxN	✓	✓	✓
Wave	4MxN	✓	✓	–
Fast Wave	3MxN	✓	✓	–

IV. Conclusions

Phase Change Memory is a promising storage class memory for modern electronic systems. However, thermal crosstalk is a major reliability issue for these memories, as technology scales down to the nanometer range and cells' proximity shortens. According to this phenomenon, when a cell is programmed, neighboring cells may experience parasitic heating, which can lead to data loss through a write disturb fault mechanism. March testing algorithms for phase change memories have been proposed in the literature, aiming to detect thermal crosstalk related write disturb faults. However, these algorithms fail to maximize the heating in the neighborhood of a cell. Thus, hard to detect write disturb faults may not be activated, leading to test escapes.

In this work, we propose efficient testing algorithms that maximize the heating in the neighborhood of each cell in the memory array through proper sequential writing operations on the immediate adjacent cells to a cell under test. Towards this direction, the Type-1 neighborhood is exploited, utilizing either the typical or the two-group tiling methods. The cells in

the deleted neighborhood (aggressor cells) of every base cell (possible victim cell) are sequentially written by programming them to the RESET state (logic 0) in order to maximize the heat transfer to the base cell, which is at the unstable amorphous (RESET) state. This way, hard to detect thermal crosstalk induced write disturb faults can be activated and detected.

The proposed testing algorithms have comparable complexity with respect to the existing ones in the open literature that target the detection of write disturb faults, being more effective to activate and cover those faults that are hard to detect.

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