Status: 24 March 2024

DATE 2024

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Foreword

Dear Colleague,

We proudly present the Advance Programme of the Design, Automation, and Test in Europe conference, DATE 2024. From the 25th to the 27th of March 2024, the community meets at the Palacio De Congresos Valencia (Valencia Conference Centre - VCC) in Spain for Europe's largest design automation conference to discuss innovative ideas in all aspects of electronic design, automation and test – from system-level hardware and software implementation, right down to integrated circuit design and new electronics devices. We warmly welcome you to this event!

DATE 2024 adopts the renewed format that was first introduced in 2023. This means that DATE 2024 leverages once again an intensive three-day format, focussing on interaction and further strengthening of our already tight-knit community. The vast majority of regular papers will be presented in technical sessions using short flash-presentations, where the emphasis is on embedded poster-supported live interactions (in addition to common full-length presentation videos available before, during and after the conference). By using this format, we make sure that the attendees can actually spend their time doing what conferences are meant for: meeting, discussing and exchanging ideas.

Main Technical Programme

The main conference programme over the three days of the conference includes **29 Interactive Technical Sessions and 4 Sessions dedicated to the presentation of Best Paper Award candidates.** All sessions are organized in parallel tracks aligned with the four areas of DATE, i.e.,

D – Design Methods & Tools,

A – Application Design,

T – Test and Dependability, and

E – Embedded Systems Design.

This year, we observed a drastic increase in paper submissions, with 19% more submissions than DATE 2023. Out of a total of 1.314 abstract submissions, 996 full research papers eventually went into review. As always, all these full papers have undergone a rigorous review procedure with the help of the 405 members of the Technical Programme Committee, who carried out 3.956 reviews (mostly four reviews per submission). As the result of this process, 244 papers (24.5%) were finally selected for regular presentation and 60 additional submissions for presentation as extended abstract. We would like to sincerely thank all members of the Technical Programme Committee for their efforts on this demanding task!

Most importantly, our thanks also belong to all authors and presenters who constitute the very foundation of DATE. Authors from the submitted papers span representatives from the three main world regions: 39.5% from Europe-Middle East-Africa, 40% from the Americas, and 20.5% from Asia. Overall, all submissions involved more than 6.100 authors from 51 different countries – a distribution that clearly demonstrates DATE's international character, global reach and impact.

Monday Keynotes

After the Opening Ceremony on Monday, a plenary keynote lecture will be offered by Robert Dimond, Fellow at Arm (UK), on "Chiplet standards: a new route to Arm-based custom silicon". The presentation will be followed by a second plenary keynote lecture by Luc Augustin, CTO of Smart Photonics (NL), on "Enlighten your designs with photonic integrated circuits". Later on, still on Monday, the IEEE CEDA Distinguished Lecturer Lunchtime Keynote will be given by Hai "Helen" Li, Clare Boothe Luce Professor and Department Chair of the Electrical and Computer Engineering Department at Duke University, on "AI Models for Edge Computing: Hardware-aware Optimizations for Efficiency". Each keynote talk is also followed by a "Later… with the keynote speakers" session to enable deeper discussion and exchanges between the speakers and the DATE community.

Focus Sessions

In addition, the program offers a range of Focus Sessions on Hot Topics, including

- Cryogenic Computing: Current status and Future Perspectives,
- Smoothing Disruption Across the Stack: Tales of Memory, Heterogeneity, and Compilers,
- Towards Large Scale Quantum Computing Design: The Quest from Automatic Methods and Tools to Integrated EDA Frameworks,
- A panel on Resilience of Deep Learning Applications: Where We Are and Where We Want To Go,
- Evolution of ML Hardware: From Technologies to Algorithms and Architectures,
- Resilient Cognitive Sensing and Inference in Distributed and Dynamic Environments,
- Formal Verification Under Resource Constraints,
- A panel on How to Attract, Train and Keep More Talent to Science & Semiconductor,
- AI for EDA, and EDA for AI, and
- Chip Design Enablement: How to Lower Barriers to Hardware Design with High Level Languages, Generative AI, and Cloud.

Two **Late Breaking Results** sessions cover novel (orthogonal) research directions and breakthrough results in a variety of DATE subdomains. There will also be presentations covering results and lessons learned from **Multi-Partner projects** addressing the full span of DATE topics. A new **DivEDA** session aims at increasing diversity in engineering broadly, and EDA in particular. As we did last year, the programme will again feature two consecutive "Unplugged" sessions to stimulate brainstorming around the theme of "Twinning Paradigm": a session format centered on direct exchanges among the participants, to formulate timely challenges as research problems and find inspiration for solution approaches.

Special Days

Two Special Days embedded in the programme will focus on areas bringing new challenges to the system design community: **Sustainable Computing** and **Responsible and Robust AI**. Each of the Special Days will have a full programme of keynotes and technical presentations.

The Special Day on **Sustainable Computing** will focus on the rapidly-increasing concern of energy consumption in the computing ecosystem: as society relies heavily on computing as a tool for science and engineering, administration, education, and even entertainment, the stark increase in compute-resources demand could make traditional information and computing technology infrastructure unsustainable. Thus, energy efficiency must become a key design parameter for computing systems and applications, at all scales. To this end, there is an urgent

need to design and deploy sustainable (super)computing systems. Despite the urgency of the problem, also highlighted by the European Green Deal policy of 2020, today there is a lack of methods and tools to develop systems that are sustainable by design. It is therefore necessary to bring together system designers, tool designers, algorithm designers, domain experts, and policy makers to address sustainability issues holistically. A highlight of this special day will be the **lunchtime keynote** given by Ayse Coskun of Boston University (USA), who will talk about "Data Center Demand Response for Sustainable Computing: Myth or Opportunity?".

The Special Day on **Responsible and Robust AI** addresses the significant prominence that AI models have gained across various domains in society, particularly in critical applications such as autonomous vehicles, banking, healthcare, and industry. To be practically and safely applicable to embedded systems, designers must develop responsible and robust AI solutions. This concept has a profound impact on integrating AI into our everyday products. Firstly, since AI will control multiple system functionalities, the models must ensure the system's robustness and security. Secondly, the decisions made by AI models can be subject to blame or credit, thus there is a need of dedicating substantial efforts to explainability and fairness, an aspect that becomes even more complex in the context of embedded systems. The objective of this Special Day is to showcase the latest advancements in the design and implementation of new models for responsible AI, considering hardware properties, as well as addressing the societal aspects related to responsible AI. As a highlight of the special day, Francisco Herrara of Granada University (Spain), will offer a **lunchtime keynote** about "Responsible Artificial Intelligence Systems: From Trustworthiness to Governance".

Special Initiative on Autonomous Systems Design

A now traditional Special Initiative on Autonomous Systems Design is held on Monday and Tuesday, consisting of reviewed and invited papers, as well as working sessions on self-governed and self-adaptive systems that are designed to operate in an open and evolving environment, which has not been completely defined at design time. Monday sessions will include a Special session on "Perception in Autonomous Systems," as well as two technical sessions on "Designing Adaptive Autonomous Systems for Resource-Constrained Platforms" and "Towards Assuring Safe Autonomous Driving". Tuesday will kick off with a technical session on "Real-Time Aware Communication Systems for Autonomy", which will be followed by a presentation by Edward Lee of UC Berkeley (USA) offering an **embedded keynote** on "Certainty or Intelligence: Pick One!". The Special Initiative will conclude with a workshop on "Autonomous Systems Certification and Homologation".

Young People Programme

The Young People Programme (YPP), an initiative targeting PhD students with the goal of supporting their career development, will take place on Monday and Tuesday. The programme kicks off on Monday afternoon with the **Careers Fair – Industry**, during which participating companies will introduce themselves and explain their business and working environment. Hereafter, PhD students will have the opportunity to introduce themselves to potential employers from the EDA and microelectronics industries, and arrange interviews during the **Speed Dating** session. An additional panel will feature young professionals from companies and startups discussing their experience in transitioning from academia to industry or a startup. During the **Careers Fair – Academia** session, researchers from academia with open positions will meet enthusiastic students who are looking for research positions in academia. Of special note is the **YPP keynote** to be provided by Matt Venn on "Give your CV the edge with open source EDA ". The **PhD Forum** will close the first day of the conference, and will include 41 selected

students who have completed, or are about to complete, their PhD thesis showcasing their work to the academic and industrial community.

On Tuesday, the Young People Programme continues with the **University Fair**, which fosters the transfer of mature academic work to a large audience by showcasing academic prototypes of software and hardware solutions in the different DATE topic fields. The YPP is concluded with the introduction and kick-off session of the **Arm Design Contest**.

Workshops

Over the course of the conference, **seven half-day workshops** cover several pressing topics from areas such as:

- Eco-ES: Eco-design and circular economy of Electronic Systems,
- 3D Integration: Heterogeneous 3D Architectures and Sensors,
- Nano Security: From Nano-Electronics to Secure Systems,
- Open-Source Design Automation,
- Hyperdimensional Computing and Vector Symbolic Architectures for Automation and Design in Technology and Systems,
- Tips and Tricks for a Successful Multi-Project-Wafer (MPW) Chip, and
- Enabling rapid and sustainable RISC-V based research using open source HW and SW.

Technical Tutorials

The DATE programme will include four embedded tutorials offered by leading experts in their respective fields. The topics span:

- Using Generative AI for Next-generation EDA,
- On-Device Continual Learning Meets Ultra-Low Power Processing,
- Coarse-Grained Reconfigurable Arrays: Modelling and Exploration Using the Open-Source CGRA-ME Framework, and
- Introduction to Certifiable General-purpose GPU Programming for Safety-Critical Systems using Khronos APIs.

Finally, the technical programme is complemented by the **Welcome Reception** on Monday evening and the traditional **DATE Party** on Tuesday evening. Both events are unique networking opportunities for the community to meet, discuss and exchange.

For further information, please visit: www.date-conference.com

Overall, this year's programme provides a broad, deep and exciting coverage of all the topics our community stands for. We sincerely thank everyone who participated in its organisation and execution. And, of course, we wish you an exciting and memorable DATE 2024!

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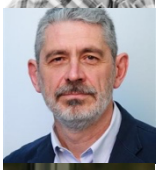

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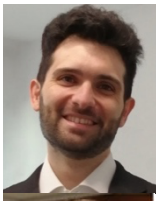

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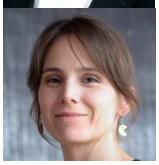

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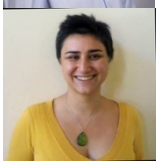

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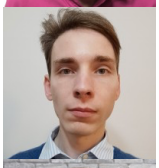

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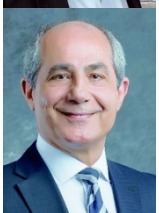

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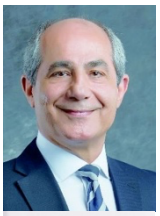

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D7 Formal Methods and Verification

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D8 Network-on-Chip and on-chip communication

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D9 Architectural and Microarchitectural Design

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D10 Low-power, Energy-efficient and Thermal-aware Design

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Oliver Keszocze, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), DE
Weiqiang Liu, Nanjing University of Aeronautics and Astronautics, CN
Veljko Pejovic, University of Ljubljana, SI
Alessandro Savino, Politecnico di Torino, IT
Florian Scheidegger, IBM Research GmbH, CH
Zdenek Vasicek, Brno University of Technology, CZ
Lan Wei, University of Waterloo, CA
Xavier Martorell, Universitat Politècnica de Catalunya, ES
Bogdan Pasca, Intel, FR
Stefania Perri, University of Calabria - DIMEG, IT
Laura Pozzi, USI Lugano, CH
Stylianos Venieris, Samsung AI, GB
Sotirios Xydis, National Technical University of Athens, GR

D13 Logical Analysis and Design

Chair: Tiziano Villa, Dipartimento d'Informatica, Universita' di Verona, IT
Co-Chair: Elena Dubrova, Royal Institute of Technology - KTH, SE
Valentina Ciriani, Universita' degli Studi di Milano, IT
Petr Fišer, Czech Technical University in Prague, FIT, CZ
Masahiro Fujita, University of Tokyo, JP
Rajeev Murgai, Synopsys India Pvt. Ltd., IN
Weikang Qian, Shanghai Jiao Tong University, CN
Andre Reis, UFRGS, BR
Eleonora Testa, Synopsys Inc., US

D14 Physical Analysis and Design

Chair: Laleh Behjat, University of Calgary, CA
Co-Chair: Shao-Yun Fang, National Taiwan University of Science and Technology, TW
Shaahin Angizi, New Jersey Institute of Technology, US
Alper Demir, Koc University, TR
Aysa Fakheri Tabrizi, University of Calgary, CA
Amin Farshidi, Cadence Design Systems, US
Matthias Fuegger, CNRS & LMF, ENS Paris-Saclay, FR
Patrick Groeneveld, DAC, US
Nima Karimpour Darav, Xilinx, Inc (AMD)., CA
Cristina Meinhardt, UFSC, BR
Renan Netto, Federal University of Santa Catarina, BR
Vojin Oklobdzija, University of California Davis, US
Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), DE
Mehmet Yildiz, Cadence Design Systems, US
Wenjian Yu, Tsinghua University, CN

D15 Emerging Design Technologies for Future Computing

Chair: Alessio Spessot, Imec, BE
Co-Chair: Vihar Georgiev, University of Glasgow, GB
Ari Alastalo, VTT, FI
Mohamed M. Sabry Aly, Nanyang Technological University, SG
Salvatore Amoroso, Synopsys Inc, GB
Veeresh Deshpande, IIT Bombay, IN
Maria Loreto Mateu Saez, Fraunhofer IIS, DE
Pierpaolo Palestri, DPIA, University of Udine, IT
Victor Sverdlov, CDL NovoMemLog IuE TUWien, AT
Aida Todri-Sanial, Eindhoven University of Technology, NL
Tony Wu, Facebook, US

D16 Emerging Design Technologies for Future Memories

Chair: Rajendra Bishnoi, Delft University of Technology, NL
Co-Chair: Jean-Philippe Noel, CEA, FR
Harshit Agarwal, IIT Jodhpur, IN
Charles Augustine, Intel Circuit Research Lab, US
Deliang Fan, Johns Hopkins University, US
Andre Guntoro, Bosch, DE
Daniele Ielmini, Poltecnico di Milano, IT
Jongsun Park, Korea University, KR
Guillaume Prenat, Spintec, FR
Fabrizio Riente, Politecnico di Torino, IT
Joachim Rodrigues, Lund University, SE
Sonal Shreya, Aarhus University, DK
William Simon, IBM, CH
Stefan Slesazeck, NaMLab gGmbH, DE
Xueyan Wang, Beihang University, CN
Tianyao Xiao, Sandia National Laboratories, US
Amirreza Yousefzadeh, University of Twente, NL

A1 Power-efficient and Sustainable Computing

Chair: Semeen Rehman, TU Wien, AT
Co-Chair: David Novo, CNRS, LIRMM, University of Montpellier, FR
David Castells-Rufas, Universitat Autònoma de Barcelona, ES
Kuan-Hsun Chen, University of Twente, NL
Yehan Ma, Shanghai Jiao Tong University, CN
Thijs Metsch, Intel, DE
Orlando Moreira, GrAI Matter Labs, NL
Mahdi Nikdast, Colorado State University, US

A2 Smart Cities, Internet of Everything, Industry 4.0

Chair: Graziano Pravadelli, University of Verona, IT
Co-Chair: Christos Kyrkou, KIOS CoE, University of Cyprus, CY
UmaMaheswari Devi, IBM Research - India, IN
Franco Fummi, University of Verona, IT
Srinivas Katkoori, University of South Florida, US
Sefki Kolozali, University of Essex, GB
Tiziana Margaria, University of Limerick and Lero, IE

Anuj Pathania, University of Amsterdam, NL
Qinru Qiu, Syracuse University, US
Ourania Spantidi, Eastern Michigan University, US
Arun Subramaniyan, Illumina Inc., US
Nishil Talati, University of Michigan, US
Ana Lucia Varbanescu, University of Amsterdam, NL
Swagath Venkataramani, IBM T. J. Watson Research Center, US
Georgios Zervakis, University of Patras, GR

A3 Automotive Systems and Smart Energy Systems

Chair: Michele Magno, ETH Zurich, CH
Co-Chair: Lulu Chan, NXP Semiconductors, NL

Donkyu Baek, Chungbuk National University, KR
Domenico Balsamo, Newcastle University, GB
Davide Brunelli, University of Trento, IT
Seonyeong Heo, Kyung Hee University, KR
Philipp Mundhenk, Robert Bosch GmbH, DE

A4 Augmented Living and Personalised Healthcare

Chair: Elisabetta Farella, Fondazione Bruno Kessler (FBK), IT
Co-Chair: Ioannis Papaefstathiou, Aristotle University of Thessaloniki, GR

Simone Benatti, University of Bologna, IT
Andrea Cossettini, ETH Zurich, CH
Amir M. Rahmani, University of California, Irvine, US

A5 Secure Systems, Circuits, and Architectures

Chair: Johanna Sepúlveda, Airbus Defence and Space, DE
Co-Chair: Cedric Marchand, Ecole centrale Lyon, FR

M. Khurram Bhatti, Information Technology University (ITU), PK
Noemie Boher, Intrinsic-ID, NL
Luca Cassano, Politecnico di Milano, IT
Ray Cheung, City University of Hong Kong, HK
Julien Francq, Naval Group, FR
Bogdan Groza, Politehnica Unviersity Timisoara, RO
Basel Halak, Southampton University, GB
Matthias Hiller, Fraunhofer AISEC, DE
Naghmeh Karimi, University of Maryland Baltimore County, US
Michail Maniatakos, New York University Abu Dhabi, AE
Sarah McCarthy, University of Waterloo, CA
Maria Méndez Real, IETR UMR CNRS 6164 Nantes Université, FR
Michael Pehl, Technical University of Munich, DE
Amin Rezaei, California State University, Long Beach, US
Jo Vliegen, ES&S, imec-COSIC, ESAT, KU Leuven, BE

A6 Self-adaptive and Context-aware Systems

Chair: Antonio Carlos Schneider Beck, Universidade Federal do Rio Grande do Sul, BR
Co-Chair: Heba Khdr, Karlsruhe Institute of Technology (KIT), DE

Antonio Miele, Politecnico di Milano, IT
Daniel Mueller-Gritschneder, Technical University of Munich, DE
Jose Nunez-Yanez, Linkoping University, SE
Behnaz Pourmohseni, Robert Bosch GmbH, DE
Amit Kumar Singh, University of Essex, GB
Lucas Wanner, Unicamp, BR
Stefan Wildermann, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), DE

A7 Applications of Emerging Technologies

Chair: Mariagrazia Graziano, Politecnico di Torino, IT
Co-Chair: Sébastien Le Beux, Concordia University, CA
Guillermo Botella, Complutense University of Madrid, ES
Yuanqing Cheng, Beihang University, CN
Giovanni Amedeo Cirillo, STMicroelectronics, IT
Florin Ciubotaru, Imec, BE
Panagiotis Dimitrakis, NCSR Demokritos, GR
Andreas Fuhrer Janett, IBM Research, CH
Georgi Gaydadjiev, Delft University of Technology / Imperial College, NL
M. Hassan Najafi, University of Louisiana at Lafayette, US
Luca Pezzarossa, Technical University of Denmark, DK
Paulina Powroznik, Silesian University of Technology, PL
Azzurra Pulimeno, Camlin Group, IT
Frank Sill Torres, German Aerospace Center, DE
Himanshu Thapliyal, University of Tennessee, US
Elena Ioana Vatajelu, TIMA, FR

A8 Industrial Experiences Brief Papers

Chair: Michelangelo Grosso, STMicroelectronics, IT
Co-Chair: Daniel Tille, Infineon Technologies, DE
Anthony Coyette, Onsemi, BE
Mohamed Ibrahim, Georgia Institute of Technology, US
Ciganda Lyl, Facultad de Ingeniería, Universidad de la República, UY
Wenjing Rao, University of Illinois at Chicago, US

Shigeru Yamashita, Ritsumeikan University, JP
Xunzhao Yin, Zhejiang University, CN

T1 Modelling and Mitigation of Defects, Faults, Variability, and Reliability

Chair: Leticia Maria Bolzani Poehls, RWTH Aachen University, DE
Co-Chair: Mottaqiallah Taouil, Delft University of Technology, NL
Hussam Amrouch, Technical University of Munich (TUM), DE
Lorena Anghel, Grenoble-Alpes University, Grenoble, France, FR
Davide Appello, Technoprobe, IT
Daniel Arumi, UPC, ES
Sarah Azimi, Politecnico di Torino, IT
Riccardo Cantoro, Politecnico di Torino, IT
Bram Kruseman, NXP Semiconductors, NL
Soumya Mittal, Qualcomm India Pvt Ltd, IN
Arnaud Virazel, LIRMM, FR

T2 Test Generation, Test Architectures, Design for Test, and Diagnosis

Chair: Maria K. Michael, Electrical and Computer Engineering & KIOS Center Excellence, U. of Cyprus, CY
Co-Chair: Grzegorz Mrugalski, Siemens EDA, PL

Paolo Bernardi, Politecnico di Torino, IT
Jennifer Dworak, Southern Methodist University, US
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Maksim Jenihhin, Tallinn University of Technology, EE
Chrysovalantis Kavousianos, Department of Computer Science and Engineering, University of Ioannina, GR
Erik Larsson, Lund University, SE
Teresa McLaurin, ARM, US
Jerzy Tyszer, Poznan University of Technology, PL

T3 Dependability and System-Level Test

Chair: Dimitris Gizopoulos, University of Athens, GR
Co-Chair: Osman Unsal, Barcelona supercomputing center, ES
Jyotika Athavale, Synopsys, US
Stefano Di Carlo, Politecnico di Torino, IT
Harish Dixit, Meta Platforms Inc., US
Sudhanva Gurumurthi, Advanced Micro Devices, Inc (AMD), US
Angeliki Kritikakou, Univ Rennes, Inria, CNRS, IRISA, FR
Jingwen Leng, Shanghai Jiao Tong University, CN

E1 Embedded Software Architecture, Compilers and Tool Chains

Chair: Sudipta Chattopadhyay, Singapore University of Technology and Design (SUTD), SG
Co-Chair: Ahmed Rezine, Linköping University, SE
Urbi Chatterjee, Indian Institute of Technology Kanpur, IN
Soumyajit Dey, IIT Kharagpur, IN
Timo Hönig, Ruhr University Bochum, DE
Michele Lora, University of Verona, IT
Hiren Patel, University of Waterloo, CA
Linh Thi Xuan Phan, University of Pennsylvania, US
Sara Royuela, Barcelona Supercomputing Center, ES
Soheil Samii, Linköping University, SE
Yi Wang, Shenzhen University, CN
Chen Yu-Fang, Academia Sinica, TW

E2 Real-time, Dependable and Privacy-Enhanced Systems

Chair: Mitra Nasri, Eindhoven University of Technology, NL
Co-Chair: Jing Li, New Jersey Institute of Technology, US
Yasmina ABDEDDAIM, Univ Gustave Eiffel, CNRS, LIGM, FR
Mohammad Ashjaei, MÃ¤lardalen University, SE
Andrea Bastoni, TUM, DE
Matthias Becker, KTH Royal Institute of Technology, SE
Gedare Bloom, University of Colorado Colorado Springs, US
Emmanuel Grolleau, LIAS, ISAE-ENSMA, Universite de Poitiers, FR
Nan Guan, City University of Hong Kong, HK
Sena Hounsinou, Metro State University, US
Zhe Jiang, University of Cambridge, GB
Federico Reghenzani, Politecnico di Milano, IT
Lei Yang, George Mason University, US

E3 Machine Learning Solutions for Embedded and Cyber-Physical Systems

Chair: Mario R. Casu, Politecnico di Torino, Department of Electronics and Telecommunications, IT
Co-Chair: Francesco Conti, University of Bologna, IT
Elnaz Ansari, Meta, US
Mladen Berekovic, Universität zu Lübeck, DE
Irem Boybat, IBM Research Europe - Zurich, CH
Anup Das, Drexel University, US

E4 Design Methodologies for Machine Learning Architectures

Chair: Smail Niar, INSA Hauts-de-France, CNRS, FR
Co-Chair: Priyadarshini Panda, Yale University, US

Giovanni Ansaloni, EPFL, CH
Riyadh Baghdadi, New York University Abu Dhabi, AE
Prabal Basu, Senior Principal Software Engineer, Cadence Design Systems, US

Kaoutar El Maghraoui, IBM, US
Maryam Hemmati, University of Auckland, NZ
Daniele Jahier Pagliari, Politecnico di Torino, IT
Axel Jantsch, TU Wien, AT
Jung-Eun Kim, Assistant professor, Computer Science, North Carolina State University, US
Hyoukjun Kwon, University of California, Irvine, US
Charles Mackin, IBM Research, US
Andres Otero, Universidad Politecnica de Madrid, ES
Hamza Ouarnoughi, INSA Hauts-de-France, FR
Işıl Öz, Izmir Institute of Technology, TR
Lirong Zheng, Fudan University, CN
Guanwen Zhong, AMD Research and Advanced Development (RAD), SG

E5 Design Modelling and Verification for Embedded and Cyber-Physical Systems

Chair: Roberto Passerone, University of Trento, IT
Co-Chair: Patricia Derler, PARC, US
Luis Almeida, University of Porto, PT
Susanne Graf, University Grenoble Alpes, CNRS, FR
Chadlia Jerad, University of Manouba, TN
Hokeun Kim, Arizona State University, US
Chung-Wei Lin, National Taiwan University, TW
Ahlem Mifdaoui, University of Toulouse- ISAE, FR

Late Breaking Results (LBR)

Chair: Aida Todri-Sanial, Eindhoven University of Technology, NL
Co-Chair: Pascal Vivet, CEA, France
Leticia Maria Bolzani Poehls, RWTH Aachen University, DE
Mario R. Casu, Politecnico di Torino, Department of Electronics and Telecommunications, IT
Valentina Ciriani, Universita' degli Studi di Milano, IT
William Fornaciari, Politecnico di Milano - DEIB, IT
Dimitris Gizopoulos, University of Athens, GR
Mariagrazia Graziano, Politecnico di Torino, IT
Daniel Grosse, Johannes Kepler University Linz, AT
Mike Hutter, PQShield, AT
Jan Moritz Joseph, RWTH Aachen University, DE
Matthias Jung, Fraunhofer IESE, DE
Maria K. Michael, Electrical and Computer Engineering & KIOS Center of Excellence, University of Cyprus, CY
Leonidas Kosmidis, Barcelona Supercomputing Center (BSC) and Universitat Politecnica de Catalunya (UPC), ES
Chung-Wei Lin, National Taiwan University, TW
Michele Lora, Universita` degli Studi di Verona, IT
Daniel Menard, INSA Rennes, FR
Antonio Miele, Politecnico di Milano, IT
Jean-Philippe Noel, CEA, FR
Bogdan Pasca, Intel, FR
Francesco Regazzoni, University of Amsterdam and ALaRI - USI, CH
Semeen Rehman, TU Wien, AT
Davide Zoni, Politecnico di Milano, IT
Hadjer Benmeziane, IBM Research, CH
José Cano, University of Glasgow, GB
Henk Corporaal, TU/e (Eindhoven University of Technology), NL
Jana Doppa, Washington State University, US
Jan Moritz Joseph, RWTH Aachen University, DE
Sheng-Chun Kao, Georgia Institute of Technology, US
Souvik Kundu, Intel Labs, US
Steven Latre, University of Antwerp - IMEC, BE
Jinho Lee, Seoul National University, KR
Huichu Liu, Facebook Inc., US
Maria Mushtaq, Telecom Paris, FR
Umit Ogras, University of Wisconsin - Madison, US
Ozcan Ozturk, Bilkent University, TR
Mazen Saghir, American University of Beirut, LB
Jae-sun Seo, Cornell Tech, US
Manan Suri, IIT-Delhi, IN
Marian Verhelst, KU Leuven, BE

DATE 2024 Technical Programme Topic Chairs

D1 System Specification and Modeling
Chair: Julio Medina, University of Cantabria, ES
Co-Chair: Matthias Jung, Universität Würzburg, DE

D2 System-Level Design Methodologies and High-Level Synthesis
Chair: Lana Josipovic, ETH Zurich, CH
Co-Chair: John Wickerson, Imperial College London, GB

D3 System Simulation and Validation
Chair: Monica Farkash, AMD, US
Co-Chair: Georg Weissenbacher, Vienna University of Technology, AT

DT4 Design and Test for Analog and Mixed-Signal Circuits and Systems, and MEMS
Chair: Helmut Graeb, Technical University of Munich, DE
Co-Chair: Rosa Rodríguez-Montañés, UPC, ES

DT5 Design and Test of Hardware Security Primitives
Chair: Mike Hutter, PQShield, AT
Co-Chair: Fatemeh Ganji, Worcester Polytechnic Institute, US

DT6 Design and Test of Secure Systems
Chair: Ricardo Chaves, INESC-ID, IST, Universidade de Lisboa, PT
Co-Chair: Elif Bilge Kavun, University of Passau, DE

D7 Formal Methods and Verification
Chair: Yakir Vizel, The Technion, IL
Co-Chair: Rolf Drechsler, University of Bremen/DFKI, DE

D8 Network-on-Chip and On-Chip Communication
Chair: Davide Zoni, Politecnico di Milano, IT
Co-Chair: Amlan Ganguly, Rochester Institute of Technology, US

D9 Architectural and Microarchitectural Design
Chair: Leonidas Kosmidis, Barcelona Supercomputing Center (BSC) and Universitat Politecnica de Catalunya (UPC), ES
Co-Chair: Paula Herber, University of Münster, DE

D10 Low-power, Energy-efficient and Thermal-aware Design
Chair: Masanori Hashimoto, Kyoto University, JP
Co-Chair: Masanori Hashimoto, Kyoto University, JP

D11 Approximate Computing
Chair: Daniel Menard, INSA Rennes, FR
Co-Chair: Anca Molnos, CEA-LIST, FR

D12 Reconfigurable Systems
Chair: Christos Bouganis, Imperial College London, GB
Co-Chair: Dionisios Pnevmatikatos, National Technical University of Athens & ICCS, GR

D13 Logical Analysis and Design
Chair: Tiziano Villa, Dipartimento d'Informatica, Universita' di Verona, IT
Co-Chair: Elena Dubrova, Royal Institute of Technology - KTH, SE

D14 Physical Analysis and Design
Chair: Laleh Behjat, University of Calgary, CA
Co-Chair: Shao-Yun Fang, National Taiwan University of Science and Technology, TW

D15 Emerging Design Technologies for Future Computing
Chair: Alessio Spessot, Imec, BE
Co-Chair: Vihar Georgiev, University of Glasgow, GB

D16 Emerging Design Technologies for Future Memories
Chair: Rajendra Bishnoi, Delft University of Technology, NL
Co-Chair: Jean-Philippe Noel, CEA, FR

A1 Power-efficient and Sustainable Computing
Chair: Semeen Rehman, TU Wien, AT
Co-Chair: David Novo, CNRS, LIRMM, University of Montpellier, FR

A2 Smart Cities, Internet of Everything, Industry 4.0
Chair: Graziano Pravadelli, University of Verona, IT
Co-Chair: Christos Kyrkou, KIOS CoE, University of Cyprus, CY

A3 Automotive Systems and Smart Energy Systems
Chair: Michele Magno, ETH Zurich, CH
Co-Chair: Lulu Chan, NXP Semiconductors, NL

A4 Augmented Living and Personalized Healthcare
Chair: Elisabetta Farella, Fondazione Bruno Kessler (FBK), IT
Co-Chair: Ioannis Papaefstathiou, Aristotle University of Thessaloniki, GR

A5 Secure Systems, Circuits, and Architectures
Chair: Johanna Sepúlveda, Airbus Defence and Space, DE
Co-Chair: Cedric Marchand, Ecole centrale Lyon, FR

A6 Self-adaptive and Context-aware Systems
Chair: Antonio Carlos Schneider Beck, Universidade Federal do Rio Grande do Sul, BR
Co-Chair: Heba Khdr, Karlsruhe Institute of Technology (KIT), DE

A7 Applications of Emerging Technologies
Chair: Mariagrazia Graziano, Politecnico di Torino, IT
Co-Chair: Sébastien Le Beux, Concordia University, CA

A8 Industrial Experiences Brief Papers
Chair: Michelangelo Grosso, STMicroelectronics s.r.l., IT
Co-Chair: Daniel Tille, Infineon Technologies, DE

T1 Modeling and Mitigation of Defects, Faults, Variability, and Reliability
Chair: Leticia Maria Bolzani Poehls, RWTH Aachen University, DE
Co-Chair: Mottaqiallah Taouil, Delft University of Technology, NL

T2 Test Generation, Test Architectures, Design for Test, and Diagnosis
Chair: Maria K. Michael, Electrical and Computer Engineering & KIOS Center of Excellence, University of Cyprus, CY
Co-Chair: Grzegorz Mrugalski, Mentor Graphics, PL

T3 Dependability and System-Level Test
Chair: Dimitris Gizopoulos, University of Athens, GR
Co-Chair: Osman Unsal, Barcelona supercomputing center, ES

DT4 Design and Test for Analog and Mixed-Signal Circuits and Systems, and MEMS
Chair: Helmut Graeb, Technical University of Munich, DE
Co-Chair: Rosa Rodríguez-Montañés, UPC, ES

DT5 Design and Test of Hardware Security Primitives
Chair: Mike Hutter, PQShield, AT
Co-Chair: Fatemeh Ganji, Worcester Polytechnic Institute, US

DT6 Design and Test of Secure Systems

Chair: Ricardo Chaves, INESC-ID, IST, Universidade de Lisboa, PT
Co-Chair: Elif Bilge Kavun, University of Passau, DE

E1 Embedded Software Architecture, Compilers and Tool Chains

Chair: Sudipta Chattopadhyay, Singapore University of Technology and Design (SUTD), SG
Co-Chair: Ahmed Rezine, Linköping University, SE

E2 Real-time, dependable and privacy-enhanced systems

Chair: Mitra Nasri, Eindhoven University of Technology, NL
Co-Chair: Jing Li, New Jersey Institute of Technology, US

E3 Machine Learning Solutions for Embedded and Cyber-Physical Systems

Chair: Mario R. Casu, Politecnico di Torino, Department of Electronics and Telecommunications, IT
Co-Chair: Francesco Conti, University of Bologna, IT

E4 Design Methodologies for Machine Learning Architectures

Chair: Smail Niar, INSA Hauts-de-France and CNRS, FR
Co-Chair: Priyadarshini Panda, Yale University, US

E5 Design modeling and verification for embedded and cyber-physical systems

Chair: Roberto Passerone, University of Trento, IT
Co-Chair: Patricia Derler, PARC, US

Late Breaking Results (LBR)

Chair: Aida Todri-Sanial, Eindhoven University of Technology, NL
Co-Chair: Pascal Vivet, CEA, FR

DATE 2024 Best Paper Awards

The **DATE 2024** best papers are:

D (&DT) Track

FusionArch: A Fusion-Based Accelerator for Point-Based Point Cloud Neural Networks

Xueyuan Liu[1]; Zhuoran Song[1]; Guohao Dai[1]; Gang Li[1]; Can Xiao[2]; Yan Xiang[2]; Dehui Kong[2]; Ke Xu[2]; Xiaoyao Liang[1],
[1]Shanghai Jiao Tong University; [2]Sanechips Technology

A Track

HW-SW Optimization of DNNs for Privacy-preserving People Counting on Low-resolution Infrared Arrays

Matteo Risso[1]; Chen Xie[1]; Francesco Daghero[1]; Alessio Burrello[1,2]; Seyedmorteza Mollaei[1]; Marco Castellano[3]; Enrico Macii[1]; Massimo Poncino[1]; Daniele Jahier Pagliari[1],
[1]Politecnico di Torino, [2]Universita di Bologna, [3]STMicroelectronics

T (&DT) Track

SELCC: Enhancing MLC Reliability and Endurance with Single Cell Error Correction Codes

Yujin Lim; Dongwhee Kim; Jungrae Kim,
Sungkyunkwan University

E Track

Efficient Exploration of Cyber-Physical System Architectures Using Contracts and Subgraph Isomorphism

Yifeng Xiao; Chanwook Oh; Michele Lora; Pierluigi Nuzzo,
University of Southern California

Best Paper Award Nominations

HW-SW Optimization of DNNs for Privacy-preserving People Counting on Low-resolution Infrared Arrays

Matteo Risso[1]; Chen Xie[1]; Francesco Daghero[1]; Alessio Burrello[1,2]; Seyedmorteza Mollaei[1]; Marco Castellano[3]; Enrico Macii[1]; Massimo Poncino[1]; Daniele Jahier Pagliari[1],
[1]Politecnico di Torino, [2]Universita di Bologna, [3]STMicroelectronics

FusionArch: A Fusion-Based Accelerator for Point-Based Point Cloud Neural Networks

Xueyuan Liu[1]; Zhuoran Song[1]; Guohao Dai[1]; Gang Li[1]; Can Xiao[2]; Yan Xiang[2]; Dehui Kong[2]; Ke Xu[2]; Xiaoyao Liang[1],
[1]Shanghai Jiao Tong University; [2]Sanechips Technology

Class-Aware Pruning for Efficient Neural Networks

Mengnan Jiang[1]; Jingcun Wang[1]; Amro Eldebiky[2]; Xunzhao Yin[3]; Cheng Zhuo[3]; Ing-Chao Lin[4]; Grace Li Zhang[1]
[1]TU Darmstadt; [2]Technical University of Munich; [3]Zhejiang University; [4]National Cheng Kung University

RVCE-FAL: A RISC-V Vector-Scalar Custom Extension for Faster FALCON Digital Signature

Xinglong Yu; Yi Sun; Yifan Zhao; Honglin Kuang; Jun Han
Fudan University

SELCC: Enhancing MLC Reliability and Endurance with Single Cell Error Correction Codes

Yujin Lim; Dongwhee Kim; Jungrae Kim,
Sungkyunkwan University

Efficient Exploration of Cyber-Physical System Architectures Using Contracts and Subgraph Isomorphism

Yifeng Xiao; Chanwook Oh; Michele Lora; Pierluigi Nuzzo,
University of Southern California

Dynamic Realization of Multiple Control Toffoli Gate

Abhoy Kole[1]; Arighna Deb[2]; Kamalika Datta[3]; Rolf Drechsler[3,1]
[1]DFKI GmbH, [2]KIIT University, [3]University of Bremen

A FeFET-based Time-Domain Associative Memory for Multi-bit Similarity Computation

Qingrong Huang[1]; Hamza Errahmouni Barkam[2]; Zeyu Yang[1]; Jianyi Yang[1]; Thomas K¨ampfe[3]; Kai Ni[4]; Grace Li Zhang[5]; Bing Li[6]; Ulf Schlichtmann[6]; Mohsen Imani[2]; Cheng Zhuo[1]; Xunzhao Yin[1]

[1]Zhejiang University, [2]University of California Irvine, [3]Fraunhofer IPMS, [4]University of Notre Dame, [5]TU Darmstadt, [6]Technical University of Munich

Scalable Sequential Optimization Under Observability Don't Cares

Dewmini Marakkalage[1]; Eleonora Testa[2]; Walter Lau Neto[3]; Alan Mishchenko[4]; Giovanni De Micheli[1]; Luca Amaru[2]

[1]EPFL, [2]Synopsys Inc., [3]University of Utah, [4]UC Berkeley

Enhancing Reliability of Neural Networks at the Edge: Inverted Normalization with Stochastic Affine Transformations

Soyed Tuhin Ahmed[1]; Kamal Danouchi[2]; Michael Hefenbrock[3]; Guillaume Prenat[2]; Lorena Anghel[2]; Mehdi Tahoori[1]

[1]Karlsruhe Institute of Technology, [2]Spintec Laboratory, [3]Revo AI

VACSEM: Verifying Average Errors in Approximate Circuits Using Simulation-Enhanced Model Counting

Chang Meng[1]; Hanyu Wang[2]; Yuqi Mai[3]; Weikang Qian[3]; Giovanni De Micheli[1]

[1]EPFL, [2]ETH Zurich, [3]Shanghai Jiao Tong University

Synthesizing Hardware-Software Leakage Contracts for RISC-V Open-Source Processors

Gideon Mohr[1]; Marco Guarnieri[2]; Jan Reineke[1]

[1]Saarland University, [2]IMDEA Software Institute

DATE 2024 Special Day on Responsible and Robust AI

AI-based systems have taken a very prominent place in all domains of activity, particularly in critical applications such as autonomous driving, banking, healthcare or industry. It is fair to say that AI systems have deeply permeated into our society. To be of practical use in embedded systems, practitioners must design responsible and robust AI. This requirement has a great impact on our daily use and interaction with this technology. First, as AI will support decision making processes, models must ensure robustness and safety against unexpected and/or adversarial inputs, i.e. they should ensure a resilient operation in the presence of faults or attacks. The second impact comes from the decision made by the AI, which could be blamed or credited for it. This point implies significant efforts on explainability and safety, this is even more complex in the context of hardware embedded models, to ensure that the algorithm performs robustly in open-world scenarios. In embedded AI, distributed and dynamic ML algorithms are of great interest to be implemented on small devices, posing additional constraints on the design of functionalities to support robustness and trustworthiness, including the precision of implementation or low power consumption rates. The goal of this special day is to showcase recent developments in the design and implementation of new techniques for robust and responsible AI, with a focus on the implications of these requirements in terms of hardware properties and specifications.

Wednesday, 27 March 2024

8:30 – 9:00

9:00 – 9:30:

ETHICAL DESIGN OF ARTIFICIAL INTELLIGENCE FOR THE INTERNET OF THINGS: A SMART HEALTHCARE PERSPECTIVE

Sudeep Pasricha (Colorado State University, US)

Summary: The dawn of the digital medicine era, ushered in by increasingly powerful Internet of Things (IoT) computing devices, is creating new therapies and biomedical solutions that promise to positively transform our quality of life. However, the integration of artificial intelligence (AI) into the digital medicine revolution also creates unforeseen and complex ethical, regulatory, and societal issues. In this talk, I will reflect on the ethical challenges facing AI-driven digital medicine. I will discuss differences between traditional ethics in the medical domain and emerging ethical challenges with AI-driven smart healthcare, particularly as they relate to transparency, bias, privacy, safety, responsibility, justice, and autonomy. Open challenges and recommendations will be outlined to enable the integration of ethical principles into the design, validation, clinical trials, deployment, monitoring, repair, and retirement of AI-based smart healthcare products.

9:30 – 10:00

TRUSTWORTHY EDGE AI – WHAT'S MISSING

Prof. Aaron Ding (TU Delft, NL)

Summary: Similar to the progression from cloud computing to cloud intelligence, we are witnessing a fast evolution from edge computing to edge intelligence (aka Edge AI). As a rising research branch that merges distributed computing, data analytics, embedded and distributed ML, Edge AI is envisioned to provide adaptation for data-driven applications and enable the creation, optimization and deployment of distributed AI/ML pipelines. However, despite of all the promises ahead, the path to realize Edge AI is far from straightforward. This talk will illustrate a major concern of Edge AI from the trustworthiness perspective, since critical building blocks are still missing. Besides practical lessons from EU SPATIAL project exploration, the talk will share an envisioned roadmap for Edge AI, which is a stepping stone to establish an appropriate foundation, on which the promise of Edge AI can be built.

11:00 – 11:30

HOW TO MAKE FEDERATED LEARNING ROBUST AND SECURE?

Aurélien Mayoue (CEA, FR)

Summary: Federated learning (FL) is a new machine learning paradigm which allows to build models in a collaborative and decentralized way. Contrary to traditional server-side approaches which aggregate data on a central server for training, FL leaves the training data distributed on the end user devices while learning a shared global model by aggregating only ephemeral locally-computed model updates. Such a decentralized optimization procedure helps to ensure data privacy and reduces communication costs as the data remains in its original location.

However, FL still faces key challenges on which a growing research effort is currently deployed: How to make the FL process fairness despite the data distribution heterogeneity across the participants? How to ensure the integrity of the federated model despite the presence of faults or malicious actors? How to secure the training process against attackers who could exploit model updates to retrieve sensitive information about participants?
In this presentation, we will start by introducing the FL process and its main key challenges. Next, we will propose solutions to address these challenges and illustrate them with use cases.

11:30 – 12:00

VALIDATION AND VERIFICATION OF AI-ENABLED VEHICLES IN THEORY AND PRACTICE

Pr. Marilyn Wolf and William Widen (University of Nebraska, US)

Summary: This talk will consider engineering methods for the evaluation of the safety of AI-enabled vehicles. We do not yet have theories and models for AI systems equivalent to those used to guide software/hardware verification and manufacturing test. However, engineers can adapt existing methods to help provide some assurance as to the safety and effectiveness of AI-enabled vehicles. We will also consider the role of management in the monitoring of validation for AI-enabled vehicles.

12:00 – 12:30

TRUSTWORTHY AI IN THALES: BEYOND PURE PERFORMANCE

Simon Fossier (Thales, FR)

Summary: Recent advances in Artificial Intelligence have opened the way to its integration in safety-critical complex systems. Designing such systems involves defining a structured process to ensure their reliability, which in turn requires to bring safety analysis to AI-based sub-components. Robustness, embeddability, formal and experimental guarantees, ethical and legal aspects – many dimensions of trustworthiness are involved in designing systems, and AI-based systems need to tackle them, despite their specificities.

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8:30 – 9:00

OPERATIONAL DESIGN DOMAIN, A KEY ELEMENT THAT CONTRIBUTES TO AI SYSTEM TRUSTWORTHINESS

Morayo Adedjouma, Research Engineer at CEA LIST (FR)

Summary: The Operational Design Domain (ODD) concept, developed in the automotive sector, makes it possible to describe the operational conditions under which an automated system or one of its functions is specifically designed to operate (inspired from SAE J3016). The objective is to define the limits of validity of the system and thus to limit the framework of its safety and validation study, recognizing that no guarantees can be provided outside its ODD. The ODD has recently attracted a lot of interest from manufacturers and it appears to be a relevant asset for the overall AI engineering workflow, including data and machine learning perspectives. However, this concept was defined with safety by design in mind. To define an AI system, the ODD is supposed to be refined throughout the development cycle of an overall system until reaching its final maturity level. Work currently carried out in Confiance.ai seeks to define this articulation, including how ODD will relevant to drive data collection and selection, machine learning evaluation, design and V&V activities.

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DATE 2024 Focus Sessions

Date: Tuesday, 26 March 2024
Time: 08:30 - 10:00 CET

FS01 Focus Session: Cryogenic Computing: Current Status And Future Perspectives

Session chair: Victor Grimblatt, Synopsys, CL
Organiser: Giovanni De Micheli, EPFL, CH

FS01.1 Depth-Optimal Addressing of 2D Qubit Array with 1D Controls

Daniel Bochen Tan, Shuohao Ping and Jason Cong, University of California, Los Angeles, US

Abstract: Reducing control complexity is essential for achieving large-scale quantum computing, particularly on platforms operating in cryogenic environments. The prospect of wiring each qubit to room-temperature control poses a challenge, as it would surpass the thermal budget in the foreseeable future. An essential tradeoff becomes evident: reducing control knobs may compromise the ability to independently address each qubit. Recent progress in neutral atom and superconductor-based quantum computing suggest that rectangular addressing may strike a balance between control granularity and flexibility for 2D qubit arrays. This scheme allows addressing qubits within a rectangle which is the product of a row and a column. While quadratically reducing controls, rectangular addressing may necessitate more depth. This problem, appeared in contexts of communication complexity, combinatorial optimization, and data mining, is NP-hard to compute or approximate. We introduce a solver based on Satisfiability Modulo Theories to achieve a depth-optimal partition. Additionally, we present a heuristic, row packing, which performs close to the optimal solver on random and synthetic benchmarks. Furthermore, we discuss rectangular partitioning in the context of fault-tolerant quantum computing, leveraging a natural two-level structure.

FS01.2 From Lindbladian to SPICE: a platform to model cryo-CMOS control for qubits

Vladimir Pesic, Andrew Wright and Edoardo Charbon, AQUA Lab, EPFL, CH

Abstract: Cryogenic classical electronics for the control of qubits can be placed near quantum processors for a more compact system, ultimately enabling a highly scalable one. However, cryogenic operation poses very strict power requirements on electronics, in addition to heavy constraints on precision in both amplitude and phase, as well as noise, so as to achieve the necessary fidelity. To test all the trade-offs that arise from these requirements, detailed simulations based on the physics of qubits and on the effects that circuits may have on them are needed. This paper focuses on the models and the simulation framework needed for quantum processors that can be efficiently executed on classical hardware. These models allow circuit design and specification derivation at all levels of the design. The suitability of the approach is demonstrated with superconducting qubit platforms and their control and characterization.

FS01.3 Technology-Aware Logic Synthesis for Superconducting Electronics

Rassul Bairamkulov, Siang-Yun Lee, Alessandro Tempia Calvino, Dewmini Marakkalage, Mingfei Yu and Giovanni De Micheli, EPFL, CH

Abstract: Superconducting electronics provide us with cryogenic digital circuits that can rival established technologies in performance and energy consumption. Today, the lack of tools for the design of large-scale integrated superconducting circuits is a major obstacle to their deployment. Few research institutions and companies have contributed to making such tools available. This review focuses on methods, algorithms, and open-source design tools for logic synthesis of superconducting circuits in two major families: single-flux quantum (SFQ) circuits and adiabatic quantum flux parametron (AQFP).

FS01.4 Challenges and Unexplored Frontiers in Electronic Design Automation for Superconducting Digital Logic

Sasan Razmkhah[1], Robert Aviles[2], Mingye li[2], Sandeep Gupta[1], Peter Beerel[2] and Massoud Pedram[2]
[1]University of Southern California (USC), US; [2]University of Southern California, US

Abstract: Positioned as a highly promising post-CMOS computing technology, superconductor electronics (SCE) offer the potential for unparalleled performance and energy efficiency gains compared to end-of-roadmap CMOS circuits. However, achieving very large-scale integration poses numerous challenges. These challenges span from the modeling and analysis of superconducting devices and logic gates to the intricate design of complex SCE circuits and systems. Addressing power and clock distribution issues, minimizing adverse effects of flux trappings, and mitigating stray electromagnetic fields in sensitive SCE circuitry are key challenges that need attention. Verification and testing of SCE circuits also remain open problems. Moreover, scaling the minimum feature sizes of SCE circuits, currently set at 150nm, presents critical scaling and physical design challenges that must be overcome. This review aims to delve into these issues, providing detailed insights while exploring existing or potential solutions to overcome them.

Date: Wednesday, 27 March 2024
Time: 11:00 - 12:30 CET

FS02 Focus Session: Smoothing Disruption Across The Stack: Tales Of Memory, Heterogeneity, And Compilers

Session chair: Ian O'Connor, École Centrale de Lyon, FR
Session co-chair: Pascal Vivet, CEA-List, FR
Organisers: Michael Niemier, University of Notre Dame, US, Ian O'Connor, École Centrale de Lyon, FR

Multiple research vectors represent possible paths to improved application-level energy and performance metrics. There are active efforts with respect to emerging logic devices, new memory technologies, novel interconnects, and heterogeneous integration architectures. Of great interest is quantifying the potential impact of a given solution to prioritize research vectors accordingly. In this session, we discuss two efforts – focused on emerging memory and heterogeneous integration technology – that speak to best practices for, and needed contributions from the design automation community to explore this vast design space. Furthermore, we highlight new research efforts that aim to develop novel compiler abstractions and frameworks that are ultimately needed to derive maximum value from new memory and/or heterogeneous and monolithic integration architectures. How compiler-focused research can play an important role with respect to design space exploration efforts will also be discussed.

FS02.1 Heterogeneous scaling driven by System-Technology Co-Optimization

Julien Ryckaert, IMEC, BE

Abstract: This talk will provide an overview of challenges and interests with respect to emerging technologies (e.g. new devices, emerging memories, 3D integration, wafer backside processing, etc.) as well as approaches to their integration in a common technology platform. It will highlight how heterogeneous scaling is aimed at addressing the growing diversity of system applications requiring large power/perfromance improvements that miniaturization cannot answer alone. It will describe the current interests in industry, research labs/consortia, and academics, and provide important context for subsequent talks.

FS02.2 Prospects and Tradeoffs for Technology-Enabled In-Memory Computing Architectures Versus Highly-Scaled CMOS Solutions

Michael Niemier[1], Zephan Enciso[1], Mohammad Mehdi Sharifi[1], X. Sharon Hu[1], Ian O'Connor[2], Nashrah Afroze[3] and Asif Khan[3]
[1]University of Notre Dame, US; [2]Lyon Institute of Nanotechnology, FR; [3]Georgia Tech, US

Abstract: This talk examines the prospects for technology-enabled, in-memory computing (IMC) architectures that may afford the potential for novel compute functionality within the memory itself, thereby obviating the need for data transfer overheads, etc. associated with more conventional architectures. While IMC has the potential to provide substantial application-level benefits with respect to figures of merit such as energy, delay, etc., it may also be challenged by issues such as the ability to reliably program and scale multi-bit memory cells, increased device variation, etc. This can in-turn impact other figures of merit such as application-level accuracy. It is also important to quantify the potential impact of technology-enabled IMC architectures to highly-scaled CMOS solutions such that industrial partners can prioritize/justify future investments with respect to specific devices. The talk will also highlight how collaborations both up-and-down the stack, and within the design automation community can facilitate these pathfinding exercises.

FS02.3 System-Technology Co-Optimization in the Era of Chiplets

Alexander Graening[1], Ravit Sharma[2] and Puneet Gupta[1]
[1]University of California, Los Angeles, US; [2]University of California at Los Angeles, US
Abstract: As conventional technology scaling becomes harder, 2.5D and 3D integration provides a viable pathway to building larger systems at lower cost. In this talk, we will describe our efforts toward building materials to algorithms cross-stack pathfinding frameworks to predict system-level power, performance and cost as a function of low-level technology changes.First, we describe a system cost modeling framework which allows for modeling of manufacturing, packaging and test costs of 2D/2.5D/3D heterogeneously integrated systems. Next, we describe an end-to-end system-technology co-optimization framework, DeepFlow, for large distributed 2.5D/3D systems, especially for the important class of distributed machine learning training applications. DeepFlow leverages a self-consistent modeling pipeline from low-level logic/memory/integration technology parameters to micro-architectures and finally to software parallelization approaches for distributed training of large language models on hundreds to thousands of accelerators. Finally, we discuss cost-performance pareto for an exemplar multi-GPU 2.5D system analyzed using these frameworks.

FS02.4 Automatic Optimization for Heterogeneous In-Memory Computing

Jeronimo Castrillon, Joao Paulo De Lima, Asif Ali Khan and Hamid Farzaneh, TU Dresden, DE
Abstract: Fuelled by exciting advances in materials and devices, in-memory computing architectures now represent a promising avenue to advance computing systems. Plenty of manual designs have already demonstrated orders of magnitude improvement in compute efficiency compared to classical Von Neumann machines in different application domains. In this talk we discuss automation flows for programming and exploring the parameter space of in-memory architectures. We report on current efforts to build an extensible framework around the MLIR compiler infrastructure to abstract from individual technologies to foster re-use. Concretely, we present optimising flows for in-memory accelerators based on crossbars, content addressable memories, and bulk-wise logic operations. We believe this kind of automation is essential to more quickly navigate the heterogeneous landscape of in-memory accelerators, and to bring the benefits of emerging architectures to a boarder range of applications.

Date: Wednesday, 27 March 2024
Time: 14:00 - 15:30 CET

FS03 Focus Session: Towards Large Scale Quantum Computing Design: The Quest From Automatic Methods And Tools To Integrated EDA Frameworks

Session chair:
Carles Hernández, TU Valencia, ES
Organisers:
Carmen G. Almudever, Technical University of Valencia, ES, Eduard Alarcon, TU Catalonia, BarcelonaTech, ES, Robert Wille, Technical University of Munich, DE, Fabio Sebastiano, Delft University of Technology, NL

Design, simulation, analysis and verification methodologies are crucial for developing electronic circuits and systems at large. Whereas long-standing EDA software is used in the semiconductor technology, there is no counterpart for quantum computing systems yet. Although the quantum computing community started utilizing and adapting some of the already existing EDA tools, for instance, to design quantum processors and control electronics for driving the qubits, or even to solve some quantum computing design tasks, they do not fully use the expertise gained over the last decades in the field of design automation. Current intermediate-scale quantum computers have been designed in an 'adhoc' manner with heterogeneous methods and tools. As we are entering the large-scale era, it is timely and key to further adopt EDA methodologies and software for quantum computing. In this hot-topic session, we will provide an overview on how full-stack quantum computing systems are being implemented nowadays and discuss which the main challenges are for transitioning from this current scenario to a comprehensive framework encompassing full automated system-wide architecting, design, simulation, verification, and test.

FS03.1 Architecting Large-Scale Quantum Computing Systems

Carmen G. Almudever[1] and Eduard Alarcon[2]
[1]TU Valencia, ES; [2]TU Catalonia, BarcelonaTech, ES
Abstract: The advances in quantum hardware with functional quantum processors integrating tens and even hundreds of noisy qubits, together with the availability of near-term quantum algorithms have allowed the development of the so-called full-stacks that bridge quantum applications with quantum devices. Up to now, intermmediate-size quantum computers have been designed in an ‘adhoc' manner, with heterogeneous methods and tools that are becoming more and more sophisticated as the complexity

of the systems is increasing. However, there is neither a standard and automated design procedure yet, nor comprehensive design flows that fully exploit the benefits of using design automation. In the coming years, having a full-fledged automatic design framework will be indispensable to address the design of large-scale quantum computing systems given their increasing complexity. In this talk, we will provide an overview of the different layers of the quantum computing full-stack and emphasize the key principles for architecting quantum computers such as codesign, optimization and benchmarking. We will then talk about the design of large-scale quantum computing systems and describe some of the open questions and challenges the quantum computing community is currently facing and for which the expertise of the EDA community will be crucial.

FS03.2 Superconducting Quantum Processors for Surface Code: Design and Analysis

Nadia Haider, Marc Beekman and Leonardo Dicarlo, TU Delft, NL

Abstract: Electronic design automation (EDA) plays a key role in advancing the field of various qubits by streamlining and optimizing the design process. In the realm of quantum applications, the reliance on microwave signals and systems spans a broad spectrum. The importance of proper electromagnetic analysis and microwave design is evident in the pursuit of groundbreaking advancements in quantum computing, particularly for large-scale, fault-tolerant quantum information processing units. This is impacting quantum processing chip design processes, particularly for superconducting based systems. In this talk, we will present an effective numerical method to analyse bus-mediated qubit-qubit couplings and two-qubit-gate speed limits in superconducting quantum processors designed for surface-code quantum error correction. Our hybrid simulation tool, combining finite-element and circuit simulation, enables the investigation of a complex chip layout with limited computational resources. We apply the simulation method to the design of Surface-17 processors, finding good agreement with the experimental realization of Surface-17.

FS03.3 Designing the cryogenic electrical interface for large-scale quantum processors

Fabio Sebastiano, TU Delft, NL

Abstract: To enable practical applications, quantum computers must scale up from the few (<1000) quantum bits (qubits) available today to the millions required for useful computations. To follow and support the scaling of the quantum processors, the complexity of the electrical interface required for controlling and reading the qubits must also grow accordingly. In particular, wiring an increasing number of cryogenic qubits to their room-temperature control electronics will soon hit a brick wall due to the sheer size of the required wires, their cost, and their reliability concerns. As an alternative to alleviate such an interconnect bottleneck, cryogenic electronics operating in close proximity to the qubtis has been proposed, but this comes with additional challenges, including the limited cooling-power budget in cryogenic refrigerators, the operation of semiconductor devices well below (<4 K) their rated operating temperature range, and the need for high performance. This talk will briefly outline the functionality and the requirements for such cryogenic electrical interface and describe the design of state-of-the-art cryogenic integrated circuits, with a specific focus on cryogenic CMOS (cryo-CMOS) technology. By reviewing the current design approaches, we will highlight hurdles and opportunities, also pointing out the needs to be addressed by the EDA community, such as the availability of quantum/classical co-simulation and co-design flows, and the distinguishing features required for the process design kits (PDK) and the design tools for cryogenic integrated circuits. Those challenges will thus define a roadmap for cryogenic electronics as a crucial enabling technology for future large-scale quantum computers.

FS03.4 Software for Quantum Computing

Robert Wille, TU Munich, DE

Abstract: In the classical computing realm, software is omnipresent and not only used to realize applications but is essential in the design of electronic circuits and systems themselves. For the quantum realm, similar developments are currently emerging. But these tools do not (yet) fully utilize experiences gained in the field of design automation over the last decades. This leaves huge potential for further improvement untapped. In fact, many of the design problems considered for quantum computing are of combinatorial and exponential nature ---a complexity with which design automation experts are quite familiar with. In this talk, a selection of design tasks is discussed, for which software and particularly design automation background can be utilized. The corresponding solutions are available through the Munich Quantum Toolkit (MQT) which offers open-source implementations for these tasks (available at https://www.cda.cit.tum.de/research/quantum/mqt). By this, an overview of the full spectrum of tasks is provided where dedicated software can be useful and, in fact, is required.

Date: Wednesday, 27 March 2024
Time: 16:30 - 18:00 CET

FS04 Focus Session: Panel On Resilience Of Deep Learning Applications: Where We Are And Where We Want To Go

Session chair: Krishnendu Chakrabarty, Arizona State University, US
Session chair: Alberto Bosio, Ecole Centrale de Lyon, FR
Organisers: Cristiana Bolchini, Politecnico di Milano, IT, Alberto Bosio, Ecole Centrale de Lyon, FR
Panellists: Annachiara Ruospo, Politecnico di Torino, IT, Paolo Rech, Università di Trento, IT, Maksim Jenihhin, Tallinn University of Technology, EE, Masanori Hashimoto, Kyoto University, JP, Luciano Ost, Loughborough University, GB, Muhammad Shafique, New York University Abu Dhabi, AE

Hardware for AI (HW-AI), similar to traditional computing hardware, is subject to hardware faults (HW faults) that can have several sources: variations in fabrication process parameters, fabrication process defects, latent defects, i.e., defects undetectable at time-zero post-fabrication testing that manifest themselves later in the field of application, silicon ageing, e.g., time-dependent dielectric breakdown, or even environmental stress, such as heat, humidity, vibration, and Single Event Upsets (SEUs) stemming from ionization. All these HW faults can cause operational failures, potentially leading to important consequences, especially for safety-critical systems. This panel aims at gathering the various contributors of this scientific community, to discuss the milestones reached so far and the future directions in the form of open challenges to be addressed. The panel format will be exploited to involve the audience (DATE community is very active on the topic) to make the conversation as inclusive as possible, to actually allow for a broader view on the matter.

Date: Monday, 25 March 2024
Time: 11:00 - 12:30 CET

FS05 Focus Session: Evolution Of Ml Hardware: From Technologies To Algorithms And Architectures

Session chair: Krishnendu Chakrabarty, Arizona State University, US
Session co-chair: Hussam Amrouch, TU Munich (TUM), DE
Organiser: Partha Pande, Washington State University, US

Training and executing emerging machine learning (ML) workloads are computationally demanding. For this reason, the industrial trend is to design specialized chips to accelerate ML workloads to efficiently process almost any kind of data, including images, text, audio, or biosensed signals. Google's Tensor Processing Unit (TPU), for instance, accelerates deep neural network (DNN) inference and training using a systolic array, a precisely timed array containing thousands of multiply-and-accumulate (MAC) units. However, there remain many open challenges with the design of energy-efficient and reliable DNN and other ML model accelerators, including technology selection, circuit design, architecture exploration, and mapping computations, data, and communication to hardware in a scalable manner. With the rising needs of advanced algorithms for large-scale data analysis and data-driven discovery, and significant growth in emerging applications from the edge to the cloud, we need low-cost, high-performance, energy-efficient, and reliable computing systems targeted for these applications. As an example, the emergence of large language models (LLMs) that rely on deep transformer neural networks and big data processing that increasingly relies on large graph neural networks, there is a need to explore new paradigms to support ultra-high throughput and energy-efficient computation, storage, and communication in the next generation of ML accelerators. The presenters will describe the most-compelling research advances and architectural breakthroughs that will contribute to closing the gap between hype and reality in ML accelerator design.

FS05.1 Algorithm to Technology Co-Optimization for CiM-based Hyperdimensional Computing

Mahta Mayahinia[1], Simon Thomann[2], Paul Genssler[3], Christopher Münch[1], Hussam Amrouch[4] and Mehdi Tahoori[1]
[1]Karlsruhe Institute of Technology, DE; [2]Chair of AI Processor Design, TU Munich (TUM), DE; [3]University of Stuttgart, DE; [4]TU Munich (TUM), DE
Abstract: Hyperdimensional computing (HDC) has been recognized as an efficient machine learning algorithm in recent years. Robustness against noise, and simple computational operations, while being limited by the memory bandwidth, make it a perfect fit for the concept of computation in memory (CiM) with emerging nonvolatile memory (NVM) technologies. For an HDC accelerator based on NVM-CiM,

there are different parameters from the algorithm all the way down to the technology that interact with each other and affecting the overall inference accuracy as well as the energy efficiency of the accelerator. Therefore, in this paper, we propose, for the first time, a full-stack co-optimization method and use it to design an HDC accelerator based on NVM-based content addressable memory (CAM). By incorporating the device manufacturing variability and co-optimizing the algorithm and hardware design, HDC inference on our proposed NVM-based CiM accelerator can reduce the energy consumption by 3.27x, while compared to the purely software-based implementation, the inference accuracy loss is merely 0.125%.

FS05.2 Accelerating Neural Networks for Large Language Models and Graph Processing with Silicon Photonics

Salma Afifi, Febin Sunny, Mahdi Nikdast and Sudeep Pasricha, Colorado State University, US

Abstract: In the rapidly evolving landscape of artificial intelligence, large language models (LLMs) and graph processing have emerged as transformative technologies for natural language processing (NLP), computer vision, and graph-structured data applications. However, the complex structures of these models pose challenges for acceleration on conventional electronic platforms. In this paper, we describe novel hardware accelerators based on silicon photonics to accelerate transformer neural networks that are used in LLMs and graph neural networks for graph data processing. Our analysis demonstrates that both hardware accelerators achieve at least 10.2× throughput improvement and 3.8× better energy efficiency over multiple state-of-the-art electronic hardware accelerators designed for LLMs and graph processing.

FS05.3 Dataflow-Aware PIM-Enabled Manycore Architecture for Deep Learning Workloads

Harsh Sharma[1], Gaurav Narang[1], Jana Doppa[1], Umit Ogras[2] and Partha Pratim Pande[1]
[1]Washington State University, US; [2]University of Wisconsin Madison, Madison, US

Abstract: Processing-in-memory (PIM) has emerged as an enabler for the energy-efficient and high-performance acceleration of deep learning (DL) workloads. Resistive random-access memory (ReRAM) is one of the most promising technologies to implement PIM. However, as the complexity of Deep convolutional neural networks (DNNs) grows, we need to design a manycore architecture with multiple ReRAM-based processing elements (PEs) on a single chip. Existing PIM-based architectures mostly focus on computation while ignoring the role of communication. ReRAM-based tiled manycore architectures often involve many Processing Elements (PEs), which need to be interconnected via an efficient on-chip communication infrastructure. Simply allocating more resources (ReRAMs) to speed up only computation is ineffective if the communication infrastructure cannot keep up with it. In this paper, we highlight the design principles of a dataflow-aware PIM-enabled manycore platform tailor-made for various types of DL workloads. We consider the design challenges with both 2.5D interposer- and 3D integration-enabled architectures.

Date: Tuesday, 26 March 2024
Time: 16:30 - 18:00 CET

FS06 Focus Session: Resilient Cognitive Sensing And Inference In Distributed And Dynamic Environments

Session chair: Kaushik Roy, Purdue University, US
Organiser: Amit Ranjan Trivedi, University of Illinois at Chicago, US

In the rapidly evolving technological era, a seamless fusion of the physical and digital realms is more critical than ever. This special session will focus on one of the recent pivotal innovations to facilitate this integration through cognitive sensing. Rather than relying on traditional sensing mechanisms that often capture excessive and potentially redundant data—leading to the challenge of the analog data deluge—cognitive sensing offers an intelligent approach. By discerning and interpreting environmental cues, it filters out the noise, ensuring only pertinent data is processed and utilized. To further leverage the abilities of cognitive sensing in distributed and dynamic environments, the special session will also focus on the bridge from cognitive sensing to neuromorphic computing and distributed inference. Distributed inference decentralizes the computation process, allowing for data-driven decisions to be made closer to the source, such as edge devices. This decentralization not only reduces latency but also ensures more efficient data processing in real-time scenarios. Neuromorphic computing, on the other hand, seeks inspiration from the human brain. By mimicking neural structures and functions, neuromorphic systems achieve unparalleled energy efficiency and processing capabilities, especially vital for real-time dynamic environments. Both of these frameworks leverage and benefit cognitive sensing by seamlessly merging sensing and inference in a unified framework over a network of inference devices. Finally, while most data-driven models act as black boxes, lacking interpretability and theoretical guarantees on prediction quality, thus creating

challenges for mission-critical applications like autonomous vehicles, the special session will also focus on uncertainty estimation at the edge where the predictive models know when they don't know. Especially, current approaches for uncertainty-aware inference, such as Bayesian neural networks (BNNs), demand excessive computations, prohibitive under time, energy, and area constraints at the edge. To overcome this critical challenge, the special session will also focus on computationally efficient uncertainty estimation at the edge so that the downstream processing is aware of prediction risks.

FS06.1 HaLo-FL: Hardware-Aware Low-Precision Federated Learning

Yeshwanth Venkatesha, Abhiroop Bhattacharjee, Abhishek Moitra and Priyadarshini Panda, Yale University, US

Abstract: Applications of federated learning involve devices with extremely limited computational resources and often with considerable heterogeneity in terms of energy efficiency, latency tolerance, and hardware area. Although low-precision training methods have demonstrated effectiveness in accommodating the device constraints in a centralized setting, their applicability in distributed learning scenarios featuring heterogeneous client capabilities has not been well explored. In this work, we design a hardware-aware low-precision federated training framework (HaLo-FL) tailored to heterogeneous resource-constrained devices. In particular, we optimize the precision for weights, activations, and errors for each client's hardware constraint using a precision selector (named HaLo-PS). To validate our approach, we propose HaLoSim, a hardware evaluation platform that enables precision reconfigurability and evaluates hardware metrics like energy, latency, and area utilization on a crossbar-based In-memory Computing (IMC) platform.

FS06.2 Cognitive Sensing for Energy-efficient Edge Intelligence

Minah Lee, Sudarshan Sharma, Wei Chun Wang, Hemant Kumawat, Nael Rahman and Saibal Mukhopadhyay, Georgia Tech, US

Abstract: Edge platforms in autonomous systems integrate multiple sensors to interpret their environment. The high-resolution and high-bandwidth pixel arrays of these sensors improve sensing quality but also generate a vast, and arguably unnecessary, volume of real-time data. This challenge, often referred to as the analog data deluge, hinders the deployment of high-quality sensors in resource-constrained environments. This paper discusses the concept of cognitive sensing, which learns to extract low-dimensional features directly from high-dimensional analog signals, thereby reducing both digitization power and generated data volume. First, we discuss design methods for analog-to-feature extraction (AFE) using mixed-signal compute-in-memory. Next, we then present examples of cognitive sensing, incorporating signal processing or machine learning, for various sensing modalities including vision, Radar, and Infrared. Subsequently, we discuss the reliability challenges in cognitive sensing, taking into account hardware and algorithmic properties of AFE. The paper concludes with discussions on future research directions in this emerging field of cognitive sensors.

FS06.3 Unearthing the Potential of Spiking Neural Networks

Sayeed Shafayet Chowdhury, Adarsh Kosta, Deepika Sharma, Marco Apolinario and Kaushik Roy, Purdue University, US

Abstract: Spiking neural networks (SNNs) are a promising avenue for machine learning with superior energy efficiency compared to traditional artificial neural networks (ANNs). Recent advances in training and input encoding have put SNNs on par with state-of-the-art ANNs in image classification. However, such tasks do not utilize the internal dynamics of SNNs fully. Notably, a spiking neuron's membrane potential acts as an internal memory, merging incoming inputs sequentially. This recurrent dynamic enables the networks to learn temporal correlations, making SNNs suitable for sequential learning. Such problems can also be tackled using ANNs. However, to capture the temporal dependencies, either the inputs have to be lumped over time (e.g. Transformers); or explicit recurrence needs to be introduced (e.g. recurrent neural networks (RNNs), long-short-term memory (LSTM) networks), which incurs considerable complexity. To that end, we explore the capabilities of SNNs in providing lightweight solutions to four sequential tasks involving text, speech and vision. Our results demonstrate that SNNs, by leveraging their intrinsic memory, can be an efficient alternative to RNNs and LSTMs for sequence processing, especially for certain edge applications. Furthermore, SNNs can be combined with ANNs (hybrid networks) synergistically to obtain the best of both worlds in terms of accuracy and efficiency.

Navigating the Unknown: Uncertainity-Aware Autonomy of Edge Robotics with Compute-in-Memory

Nastaran Darabi[1], Priyesh Shukla[2], Dinithi Jayasuriya[1], Divake Kumar[1], Alex Stutts[1] and Amit Trivedi[1]
[1]University of Illinois at Chicago, US; [2]Samsung, IN

Abstract: This paper addresses the challenging problem of energy-efficient and uncertainty-aware pose estimation in insect-scale drones, which is crucial for tasks such as surveillance in constricted spaces and

for enabling non-intrusive spatial intelligence in smart homes. Since tiny drones operate in highly dynamic environments, where factors like lighting and human movement impact their predictive accuracy, it is crucial to deploy uncertainty-aware prediction algorithms that can account for environmental variations and express not only the prediction but also confidence in the prediction. We address both of these challenges with Compute-in-Memory (CIM) which has become a pivotal technology for deep learning acceleration at the edge. While traditional CIM techniques are promising for energy-efficient deep learning, to bring in the robustness of uncertainty-aware predictions at the edge, we introduce a suite of novel techniques: First, we discuss CIM-based acceleration of Bayesian filtering methods uniquely by leveraging the Gaussian-like switching current of CMOS inverters along with co-design of kernel functions to operate with extreme parallelism and with extreme energy efficiency. Secondly, we discuss the CIM-based acceleration of variational inference of deep learning models through probabilistic processing while unfolding iterative computations of the method with a compute reuse strategy to significantly minimize the workload. Overall, our co-design methodologies demonstrate the potential of CIM to improve the processing efficiency of uncertainty-aware algorithms by orders of magnitude, thereby enabling edge robotics to access the robustness of sophisticated prediction frameworks within their extremely stringent area/power resources.

Date: Monday, 25 March 2024
Time: 16:30 - 18:00 CET

FS07 Focus Session: Formal Verification Under Resource Constraints

Session chair: Rolf Drechsler, University of Bremen | DFKI, DE
Organiser: Lukas Sekanina, Brno University of Technology, CZ

Formal verification is almost always connected with constrained resources, e.g., the runtime of a given formal verification technique is constrained by available time or resources, or a verification technique can have some principal applicability constraints. The role of constraints thus becomes crucial and, in fact, determines whether a formal verification technique can be applied or not. The objective of this proposal is to (a) present current trends in formal verification methods working under various resource constraints, (b) highlight successful results, and (c) discuss possible future developments.

FS07.1 Polynomial Formal Verification of Sequential Circuits

Caroline Dominik[1] and Rolf Drechsler[2]
[1]Institute of Computer Science, University of Bremen/DFKI, DE; [2]University of Bremen | DFKI, DE
Abstract: Recently, the concept of Polynomial Formal Verification (PFV) has been introduced and successfully applied to several classes of functions, allowing complete verification under resource constraints. But so far, all studies were carried out for combinational circuits only. In this paper we show how the concept of PFV can be extended to sequential circuits. As a first case study we show for counters that PFV can be performed, even though they have an exponential number of states, i.e., they can be fully formally verified within polynomial upper bounds on run-time and memory requirement.

FS07.2 Automated Verifiability-Driven Design of Approximate Circuits: Exploiting Error Analysis

Zdenek Vasicek, Vojtech Mrazek and Lukas Sekanina, Brno University of Technology, CZ
Abstract: A fundamental assumption for search-based circuit approximation methods is the ability to massively and efficiently traverse the search space and evaluate candidate solutions. For complex approximate circuits (adders and multipliers), common error metrics, and error analysis approaches (SAT solving, BDD analysis), we perform a detailed analysis to understand the behavior of the error analysis methods under constrained resources, such as limited execution time. In addition, we show that when evaluating the error of a candidate approximate circuit, it is highly beneficial to reuse knowledge obtained during the evaluation of previous circuit instances to reduce the total design time. When an adaptive search strategy that drives the search towards promptly verifiable approximate circuits is employed, the method can discover circuits that exhibit better trade-offs between error and desired parameters (such as area) than the same method with unconstrained verification resources and within the same overall time budget. For 16-bit and 20-bit approximate multipliers, it was possible to achieve a 75\% reduction in area when compared with the baseline method.

FS07.3 Using Formal Verification Methods for Optimization of Circuits under External Constraints

Daniel Grosse, Lucas Klemmer and Dominik Bonora, Johannes Kepler University Linz, AT

Abstract: This paper targets the optimization of circuit netlists by eliminating redundant gates under given external constraints. Typical examples for external constraints – which can be viewed as external don't cares – are restrictions on input operands, instruction subsets used by a processor for specific applications, or limited operation modes of an integrated IP block. Targeting external don't cares presents a challenge because the optimization problem changes from a completely specified Boolean function to a Boolean relation. We propose an optimization approach that utilizes formal verification methods. We demonstrate how to formulate Property Checking (PC) and Equivalence Checking (EC) problems to determine if a gate is redundant under given external constraints. Essentially, the validity of up to four rules must be checked per gate. We show that these checks can be solved concurrently, resulting in faster overall optimization. We have implemented our approach as the tool Formal SYNthesis (FSYN). FSYN utilizes open-source tools to scale the solving of formal instances with available hardware resources. We demonstrate that our approach can achieve substantial reductions in the number of gates for combinational circuits under given external constraints.

FS07.4 Combining Formal Verification and Testing for Debugging of Arithmetic Circuits

Jiteshri Dasari and Maciej Ciesielski, University of Massachusetts Amherst, US

Abstract: Formal verification has been successfully used to verify different types of digital circuits, including combinational and sequential logic, arithmetic circuits, and datapath designs. However, the verification techniques concentrate on confirming whether the circuit performs its intended function, while the issue of debugging, i.e., detection and correction of functional errors of the design, remains an open problem. Elaborate testing techniques have been developed that target certain types of manufacturing faults but there are no general techniques that address the debugging issue for functional bugs. This paper addresses the issue of debugging of arithmetic circuits that due to their large size and complexity are particularly hard to verify and debug. Current debugging techniques handle only simple types of bugs: gate replacement, wrong gate polarity, or a missing gate, but cannot handle more realistic faults, such as wrong wiring or using a wrong combination of logic gates. We describe a novel method that combines formal verification and testing techniques to enable efficient identification and correction of faults. The technique involves setting select signals to some predefined constants to reduce the design to easily verifiable circuit components; these components are then verified using logic equivalence checking and SAT tools. The fault can then be identified in form or a small logic area (with a few logic gates) to be replaced by a new, functionally correct logic. The proposed technique is illustrated with debugging of different types of divider circuits up to 1024 bit-wide.

Date: Tuesday, 26 March 2024
Time: 11:00 - 12:30 CET

FS08 Panel session: How to Attract, Train and Keep more Talent to Science & Semiconductor

Session chair: Catherine Le Lan, Synopsys, FR
Organisers: Catherine Le Lan, Synopsys, FR; Olivier Sentieys, Inria, FR

The microelectronics landscape is evolving, currently driven by AI and the adoption of the chiplets. With chips being an integral part of our daily lives, there is a crucial emphasis on the computing power, security, safety, and efficiency of chips. To address the future semiconductor demand and fuel a pipeline of skilled talent, this session aims to discuss strategies that unite the broader microelectronics ecosystem to collaboratively address workforce development needs.

Cultivating a Diverse Workforce to Meet EU Chips Act Ambitions

Laith Altimime, SEMI Europe, DE

Abstract: Talent remains as one of the industry's most pressing global challenge. To achieve the EU Chips Act Ambitions by achieving 20% of the global market share by 2030 we will need to more than double the current workforce in Europe and with more diverse skills. We will need to explore new strategies to Scale-Up initiatives to populate the talent pipeline. Strategies include scaled-up funding mechanisms at national and global levels by establishing global and regional Industry – Academia partnerships with focus on Diversity, Upskilling, Reskilling and Retention of the future workforce, as well as collaborative global initiatives to attract and facilitate talent mobility for a diverse international workforce.

European University Training for Chip Act: Diversity, Internationalization, Collaboration

Mehdi B. Tahoori, Karlsruhe Institute of Technology (KIT), DE

Abstract: Workforce education, training, and retention in European universities are paramount for the success of the EU Chip Act, facilitating a thriving chip design and manufacturing ecosystem in Europe. Central to this endeavor is the attraction of global talent, achieved through strategic initiatives like internationalization and the promotion of diversity. Establishing an inclusive, discrimination-free environment is pivotal in cultivating an atmosphere conducive to international scholars, both during their academic pursuits and when selecting their career paths within European industries. From a technical perspective, industry-relevant educational programs in chip design and university-industry research collaboration play indispensable roles in attracting, educating, and retaining students at both MS and PhD levels, ensuring they possess the necessary competence in chip design.

Meeting Industry Needs for Tomorrow's Chip Design Work Force

Yervant Zorian, Synopsys, US

Abstract: As chip design requirements continue to change, tomorrow's work force needs to perform new types of activities and require corresponding preparation. A well-defined collaboration between academia and chip design industry is necessary to prepare tomorrow workforce during its education stage, in order to utilize advanced ML-based EDA tools, embedded firmware, high performance interface IP subsystems, chiplets for 2.5/3D multi-die designs. This presentation will cover a particular educational model developed by Synopsys Armenia Educational Department to prepare for tomorrow's work force and implemented in partnership with several academic institutions.

How to Ensure Existing Engineers are Trained on Tomorrow's Challenges?

Peter Groos, Cadence Design Systems, DE

Abstract: The increasing demand for engineers in the semiconductor industry in the next 5 to 10 years requires strategies and programs including national or regional funding to reduce the workforce and educational gap. The effect of these programs is rather mid to long term and yet to be proven. Under the assumption that the shortage will prevail measures need to be taken to continuously develop and maintain the knowledge and skill set of today's engineering teams to create future products and solutions in the most efficient ways. Work force development programs help to develop new skills through re-skilling or up-skilling. Furthermore, prediction of market trends and agility to adopt to new demands are key in having the right skill sets when they are needed. For a successful implementation these programs need to be centered around the individual embedded in an inclusive team culture.

Date: Wednesday, 27 March 2024
Time: 8:30 - 10:00 CET

FS09 Focus session: AI for EDA, and EDA for AI

Session chair: Anuj Pathania, University of Amsterdam, NL
Session co-chair: Todor Stefanov, Leiden University, NL
Organisers: Catherine Le Lan, Synopsys, FR; Olivier Sentieys, Inria, FR

AI – The Next Revolution in Chip Design Automation

Tobias Bjerregaard, Synopsys, DK

Abstract: AI is making great strides and in particularly the generative AI technologies are set to transform entire industries. AI-based chip design flows are not only yielding better results, but also improving designer productivity by automating many of the tasks traditionally done by human experts. In this talk I will outline key uses of AI in the chip design process. I will look across the entire EDA stack at where AI-based approaches have made the highest impact. I will also look at how generative AI technologies can help capture human knowhow and as such be particularly powerful in mitigating the talent gap that the chip design industry is facing.

Automation in Deep Learning and Hardware Integration

Dolly Sapra, University Van Amsterdam, NL

Abstract: This talk focuses on how EDA tools are changing the way deep learning models are integrated with hardware, especially in edge devices. Tools to automatically identify the most suitable deep learning models for specific hardware configurations are discussed. These methods are crucial for a large number of edge devices, where limitations in power and processing capacity are often encountered. The talk further elaborates on the methods to achieve efficient system-resource management, ensuring that neural

network layers are meticulously mapped to the most appropriate hardware components. This approach not only enhances the computational efficiency of edge devices but also contributes significantly to their energy conservation. The aim of this talk is to highlight the developments and opportunities of automating deep learning inference, at a time when AI is increasingly present in every aspect of our lives and becoming integral to the devices we use every day.

Designing the future chips: A-DECA synergizes AI and Optimization techniques for Automatic Architecture Exploration

Lilia Zaourar, CEA LIST, FR

Abstract: Nowadays, chip designers face various challenges due to the short time to market, increased system complexity, computing heterogeneity, and various SW/HW constraints. Usually, traditional solutions are based on prior engineering experience from computer architects. However, finding a suitable architecture that can accommodate a good balance between various Key Performance Indicators is a notorious problem because of two issues: 1) design space is extremely large, and its size grows exponentially when adding new components, and 2) computing cost is large, in particular for metrics evaluation. A-DECA (Automated Design space Exploration for Computing Architectures) framework leverages various Combinatorial Optimization techniques and Machine Learning strategies to achieve an efficient trade-off on the usual PPA (Performance, Power, Area) but also includes other ones such as security and sustainability. A concrete use case focusing on the design of the next generation of exascale processors for HPC will be presented.

Date: Monday, 25 March 2024
Time: 14:00 - 15:30 CET

FS10 Focus session: Chip Design Enablement: How to lower barriers to hardware design with high level languages, generative AI, and Cloud

Session chair: Olivier Sentieys, Inria, FR
Organisers: Catherine Le Lan, Synopsys, FR; Olivier Sentieys, Inria, FR

Writing software to elaborate hardware (SpinalHDL)

Charles Papon, Independent, CH

Abstract: This talk will provide an overview about how software approaches can be used to capture hardware specifications and generate their corresponding Verilog/VHDL "netlist ». The main motivation for such approach being to go beyond what the System-Verilog and VHDL tooling support in terms of hardware elaboration, increasing developer productivity, being able to build hardware generation abstractions while keeping full control over the generated hardware. Another motivation is also to be able to use an extendable tool, meaning, not having to restrict yourself to baked-in features, but instead being able to extend the scope of the tool, avoiding having to switch between different languages, and so avoiding a flow fracture or mismatch. This talk will be based around the recents developments made on VexiiRiscv (a RISC-V multi-issue processor softcore), including its hardware pipelining API and scheduler generation which are based on Scala (a general purpose programming language) and SpinalHDL (a Scala library providing a hardware description API).

VeriHDL: Enforcing Correctness in LLM-Generated HDL

Valerio Tenace and Pierre-Emmanuel Gaillardon, PrimisAI, US

Abstract: Over the past few months, the rapid proliferation of Large Language Models (LLMs) for Hardware Description Language (HDL) generation has attracted considerable attention. These technologies, by automating complex design tasks, aim to streamline workflows and hasten the innovation process. However, the intrinsic probabilistic nature of LLMs introduces a degree of uncertainty, often manifesting as errors or hallucinations in the generated HDL code—a matter of great concern in the realm of hardware design where accuracy is non-negotiable. To tackle this issue, we present VeriHDL, a novel LLM-based framework tailored to bolster the accuracy and dependability of HDL code produced by generative artificial intelligence. Central to VeriHDL is a harmonious blend of sophisticated and interconnected LLMs that enable: (1) a systematic HDL generation process that leverages a dedicated knowledge base of pre-defined and verified IPs as an initial safeguard against most common mistakes, (2) an automated and iterative testbench generation mechanism, to enforce functional correctness, and (3) a seamless interface with Electronic Design Automation tools, as to enable an automatic verification process with no-human-in-the-loop. This innovative and original approach, currently in its early beta stage within PrimisAI's RapidGPT platform, is not only meant to improve the accuracy of generated code, but also to significantly reduce the time and resources required for verification. As a result, VeriHDL represents a substantial paradigm shift in hardware design, facilitating a more efficient, reliable, and

streamlined development process. In this presentation, we will delve into the foundational principles of VeriHDL, starting with an in-depth analysis of its architecture. We will then explore the dynamic interplay among its components, illustrating how they collectively contribute to the framework's effectiveness. The session will culminate in a demonstration, showcasing VeriHDL's practical application and its impact on streamlining the hardware design process.

CUMULUS: A Cloud-Based EDA Platform for Teaching and Research

Phillip Christie, Trinity College Dublin, IE

Abstract: In this presentation, I will relate our early experiences in the development and deployment of a cloud-based Electronic Design Automation (EDA) platform in Microsoft Azure, to be used as the basis of a set of laboratories associated with a Masters' degree level module in microelectronics at Trinity College Dublin. The intent of the CUMULUS platform is not to implement a commercial design flow but rather to permit students to see how choices made at one stage affect performance at later stages. The flow from device model, library characterization, synthesis, place and route, to timing analysis creates a sequence of data files in standardized formats which, while being mostly text-based, are not designed for human assessment. A key design concept of the CUMULUS platform has therefore been to use a suite of specially created MATLAB toolboxes to visualise and assess these data (in liberty, LEF, DEF, timing reports, GDSII formats) generated at each stage. This presentation will end by providing an overview of costs for the lab, show examples of the graphical representation of data files and make recommendations for future improvements to the CUMULUS platform.

DATE 2024 Focus Sessions

Date: Tuesday, 26 March 2024
Time: 08:30 - 10:00 CET

FS01 Focus Session: Cryogenic Computing: Current Status And Future Perspectives

Session chair: Victor Grimblatt, Synopsys, CL
Organiser: Giovanni De Micheli, EPFL, CH

FS01.1 Depth-Optimal Addressing of 2D Qubit Array with 1D Controls

Daniel Bochen Tan, Shuohao Ping and Jason Cong, University of California, Los Angeles, US

Abstract: Reducing control complexity is essential for achieving large-scale quantum computing, particularly on platforms operating in cryogenic environments. The prospect of wiring each qubit to room-temperature control poses a challenge, as it would surpass the thermal budget in the foreseeable future. An essential tradeoff becomes evident: reducing control knobs may compromise the ability to independently address each qubit. Recent progress in neutral atom and superconductor-based quantum computing suggest that rectangular addressing may strike a balance between control granularity and flexibility for 2D qubit arrays. This scheme allows addressing qubits within a rectangle which is the product of a row and a column. While quadratically reducing controls, rectangular addressing may necessitate more depth. This problem, appeared in contexts of communication complexity, combinatorial optimization, and data mining, is NP-hard to compute or approximate. We introduce a solver based on Satisfiability Modulo Theories to achieve a depth-optimal partition. Additionally, we present a heuristic, row packing, which performs close to the optimal solver on random and synthetic benchmarks. Furthermore, we discuss rectangular partitioning in the context of fault-tolerant quantum computing, leveraging a natural two-level structure.

FS01.2 From Lindbladian to SPICE: a platform to model cryo-CMOS control for qubits

Vladimir Pesic, Andrew Wright and Edoardo Charbon, AQUA Lab, EPFL, CH

Abstract: Cryogenic classical electronics for the control of qubits can be placed near quantum processors for a more compact system, ultimately enabling a highly scalable one. However, cryogenic operation poses very strict power requirements on electronics, in addition to heavy constraints on precision in both amplitude and phase, as well as noise, so as to achieve the necessary fidelity. To test all the trade-offs that arise from these requirements, detailed simulations based on the physics of qubits and on the effects that circuits may have on them are needed. This paper focuses on the models and the simulation framework needed for quantum processors that can be efficiently executed on classical hardware. These models allow circuit design and specification derivation at all levels of the design. The suitability of the approach is demonstrated with superconducting qubit platforms and their control and characterization.

FS01.3 Technology-Aware Logic Synthesis for Superconducting Electronics

Rassul Bairamkulov, Siang-Yun Lee, Alessandro Tempia Calvino, Dewmini Marakkalage, Mingfei Yu and Giovanni De Micheli, EPFL, CH

Abstract: Superconducting electronics provide us with cryogenic digital circuits that can rival established technologies in performance and energy consumption. Today, the lack of tools for the design of large-scale integrated superconducting circuits is a major obstacle to their deployment. Few research institutions and companies have contributed to making such tools available. This review focuses on methods, algorithms, and open-source design tools for logic synthesis of superconducting circuits in two major families: single-flux quantum (SFQ) circuits and adiabatic quantum flux parametron (AQFP).

FS01.4 Challenges and Unexplored Frontiers in Electronic Design Automation for Superconducting Digital Logic

Sasan Razmkhah[1], Robert Aviles[2], Mingye li[2], Sandeep Gupta[1], Peter Beerel[2] and Massoud Pedram[2]
[1]University of Southern California (USC), US; [2]University of Southern California, US

Abstract: Positioned as a highly promising post-CMOS computing technology, superconductor electronics (SCE) offer the potential for unparalleled performance and energy efficiency gains compared to end-of-roadmap CMOS circuits. However, achieving very large-scale integration poses numerous challenges. These challenges span from the modeling and analysis of superconducting devices and logic gates to the intricate design of complex SCE circuits and systems. Addressing power and clock distribution issues, minimizing adverse effects of flux trappings, and mitigating stray electromagnetic fields in sensitive SCE circuitry are key challenges that need attention. Verification and testing of SCE circuits also remain open problems. Moreover, scaling the minimum feature sizes of SCE circuits, currently set at 150nm, presents critical scaling and physical design challenges that must be overcome. This review aims to delve into these issues, providing detailed insights while exploring existing or potential solutions to overcome them.

Date: Wednesday, 27 March 2024
Time: 11:00 - 12:30 CET

FS02 Focus Session: Smoothing Disruption Across The Stack: Tales Of Memory, Heterogeneity, And Compilers

Session chair: Ian O'Connor, École Centrale de Lyon, FR
Session co-chair: Pascal Vivet, CEA-List, FR
Organisers: Michael Niemier, University of Notre Dame, US, Ian O'Connor, École Centrale de Lyon, FR

Multiple research vectors represent possible paths to improved application-level energy and performance metrics. There are active efforts with respect to emerging logic devices, new memory technologies, novel interconnects, and heterogeneous integration architectures. Of great interest is quantifying the potential impact of a given solution to prioritize research vectors accordingly. In this session, we discuss two efforts – focused on emerging memory and heterogeneous integration technology – that speak to best practices for, and needed contributions from the design automation community to explore this vast design space. Furthermore, we highlight new research efforts that aim to develop novel compiler abstractions and frameworks that are ultimately needed to derive maximum value from new memory and/or heterogeneous and monolithic integration architectures. How compiler-focused research can play an important role with respect to design space exploration efforts will also be discussed.

FS02.1 Heterogeneous scaling driven by System-Technology Co-Optimization

Julien Ryckaert, IMEC, BE

Abstract: This talk will provide an overview of challenges and interests with respect to emerging technologies (e.g. new devices, emerging memories, 3D integration, wafer backside processing, etc.) as well as approaches to their integration in a common technology platform. It will highlight how heterogeneous scaling is aimed at addressing the growing diversity of system applications requiring large power/perfromance improvements that miniaturization cannot answer alone. It will describe the current interests in industry, research labs/consortia, and academics, and provide important context for subsequent talks.

FS02.2 Prospects and Tradeoffs for Technology-Enabled In-Memory Computing Architectures Versus Highly-Scaled CMOS Solutions

Michael Niemier[1], Zephan Enciso[1], Mohammad Mehdi Sharifi[1], X. Sharon Hu[1], Ian O'Connor[2], Nashrah Afroze[3] and Asif Khan[3]
[1]University of Notre Dame, US; [2]Lyon Institute of Nanotechnology, FR; [3]Georgia Tech, US

Abstract: This talk examines the prospects for technology-enabled, in-memory computing (IMC) architectures that may afford the potential for novel compute functionality within the memory itself, thereby obviating the need for data transfer overheads, etc. associated with more conventional architectures. While IMC has the potential to provide substantial application-level benefits with respect to figures of merit such as energy, delay, etc., it may also be challenged by issues such as the ability to reliably program and scale multi-bit memory cells, increased device variation, etc. This can in-turn impact other figures of merit such as application-level accuracy. It is also important to quantify the potential impact of technology-enabled IMC architectures to highly-scaled CMOS solutions such that industrial partners can prioritize/justify future investments with respect to specific devices. The talk will also highlight how collaborations both up-and-down the stack, and within the design automation community can facilitate these pathfinding exercises.

FS02.3 System-Technology Co-Optimization in the Era of Chiplets

Alexander Graening[1], Ravit Sharma[2] and Puneet Gupta[1]
[1]University of California, Los Angeles, US; [2]University of California at Los Angeles, US
Abstract: As conventional technology scaling becomes harder, 2.5D and 3D integration provides a viable pathway to building larger systems at lower cost. In this talk, we will describe our efforts toward building materials to algorithms cross-stack pathfinding frameworks to predict system-level power, performance and cost as a function of low-level technology changes.First, we describe a system cost modeling framework which allows for modeling of manufacturing, packaging and test costs of 2D/2.5D/3D heterogeneously integrated systems. Next, we describe an end-to-end system-technology co-optimization framework, DeepFlow, for large distributed 2.5D/3D systems, especially for the important class of distributed machine learning training applications. DeepFlow leverages a self-consistent modeling pipeline from low-level logic/memory/integration technology parameters to micro-architectures and finally to software parallelization approaches for distributed training of large language models on hundreds to thousands of accelerators. Finally, we discuss cost-performance pareto for an exemplar multi-GPU 2.5D system analyzed using these frameworks.

FS02.4 Automatic Optimization for Heterogeneous In-Memory Computing

Jeronimo Castrillon, Joao Paulo De Lima, Asif Ali Khan and Hamid Farzaneh, TU Dresden, DE
Abstract: Fuelled by exciting advances in materials and devices, in-memory computing architectures now represent a promising avenue to advance computing systems. Plenty of manual designs have already demonstrated orders of magnitude improvement in compute efficiency compared to classical Von Neumann machines in different application domains. In this talk we discuss automation flows for programming and exploring the parameter space of in-memory architectures. We report on current efforts to build an extensible framework around the MLIR compiler infrastructure to abstract from individual technologies to foster re-use. Concretely, we present optimising flows for in-memory accelerators based on crossbars, content addressable memories, and bulk-wise logic operations. We believe this kind of automation is essential to more quickly navigate the heterogeneous landscape of in-memory accelerators, and to bring the benefits of emerging architectures to a boarder range of applications.

Date: Wednesday, 27 March 2024
Time: 14:00 - 15:30 CET

FS03 Focus Session: Towards Large Scale Quantum Computing Design: The Quest From Automatic Methods And Tools To Integrated EDA Frameworks

Session chair: Carles Hernández, TU Valencia, ES
Organisers:
Carmen G. Almudever, Technical University of Valencia, ES, Eduard Alarcon, TU Catalonia, BarcelonaTech, ES, Robert Wille, Technical University of Munich, DE, Fabio Sebastiano, Delft University of Technology, NL

Design, simulation, analysis and verification methodologies are crucial for developing electronic circuits and systems at large. Whereas long-standing EDA software is used in the semiconductor technology, there is no counterpart for quantum computing systems yet. Although the quantum computing community started utilizing and adapting some of the already existing EDA tools, for instance, to design quantum processors and control electronics for driving the qubits, or even to solve some quantum computing design tasks, they do not fully use the expertise gained over the last decades in the field of design automation. Current intermediate-scale quantum computers have been designed in an 'adhoc' manner with heterogeneous methods and tools. As we are entering the large-scale era, it is timely and key to further adopt EDA methodologies and software for quantum computing. In this hot-topic session, we will provide an overview on how full-stack quantum computing systems are being implemented nowadays and discuss which the main challenges are for transitioning from this current scenario to a comprehensive framework encompassing full automated system-wide architecting, design, simulation, verification, and test.

FS03.1 Architecting Large-Scale Quantum Computing Systems

Carmen G. Almudever[1] and Eduard Alarcon[2]
[1]TU Valencia, ES; [2]TU Catalonia, BarcelonaTech, ES
Abstract: The advances in quantum hardware with functional quantum processors integrating tens and even hundreds of noisy qubits, together with the availability of near-term quantum algorithms have allowed the development of the so-called full-stacks that bridge quantum applications with quantum devices. Up to now, intermmediate-size quantum computers have been designed in an ‘adhoc' manner, with heterogeneous methods and tools that are becoming more and more sophisticated as the complexity of the systems is increasing. However, there is neither a standard and automated design procedure yet,

nor comprehensive design flows that fully exploit the benefits of using design automation. In the coming years, having a full-fledged automatic design framework will be indispensable to address the design of large-scale quantum computing systems given their increasing complexity. In this talk, we will provide an overview of the different layers of the quantum computing full-stack and emphasize the key principles for architecting quantum computers such as codesign, optimization and benchmarking. We will then talk about the design of large-scale quantum computing systems and describe some of the open questions and challenges the quantum computing community is currently facing and for which the expertise of the EDA community will be crucial.

FS03.2 Superconducting Quantum Processors for Surface Code: Design and Analysis

Nadia Haider, Marc Beekman and Leonardo Dicarlo, TU Delft, NL

Abstract: Electronic design automation (EDA) plays a key role in advancing the field of various qubits by streamlining and optimizing the design process. In the realm of quantum applications, the reliance on microwave signals and systems spans a broad spectrum. The importance of proper electromagnetic analysis and microwave design is evident in the pursuit of groundbreaking advancements in quantum computing, particularly for large-scale, fault-tolerant quantum information processing units. This is impacting quantum processing chip design processes, particularly for superconducting based systems. In this talk, we will present an effective numerical method to analyse bus-mediated qubit-qubit couplings and two-qubit-gate speed limits in superconducting quantum processors designed for surface-code quantum error correction. Our hybrid simulation tool, combining finite-element and circuit simulation, enables the investigation of a complex chip layout with limited computational resources. We apply the simulation method to the design of Surface-17 processors, finding good agreement with the experimental realization of Surface-17.

FS03.3 Designing the cryogenic electrical interface for large-scale quantum processors

Fabio Sebastiano, TU Delft, NL

Abstract: To enable practical applications, quantum computers must scale up from the few (<1000) quantum bits (qubits) available today to the millions required for useful computations. To follow and support the scaling of the quantum processors, the complexity of the electrical interface required for controlling and reading the qubits must also grow accordingly. In particular, wiring an increasing number of cryogenic qubits to their room-temperature control electronics will soon hit a brick wall due to the sheer size of the required wires, their cost, and their reliability concerns. As an alternative to alleviate such an interconnect bottleneck, cryogenic electronics operating in close proximity to the qubtis has been proposed, but this comes with additional challenges, including the limited cooling-power budget in cryogenic refrigerators, the operation of semiconductor devices well below (<4 K) their rated operating temperature range, and the need for high performance. This talk will briefly outline the functionality and the requirements for such cryogenic electrical interface and describe the design of state-of-the-art cryogenic integrated circuits, with a specific focus on cryogenic CMOS (cryo-CMOS) technology. By reviewing the current design approaches, we will highlight hurdles and opportunities, also pointing out the needs to be addressed by the EDA community, such as the availability of quantum/classical co-simulation and co-design flows, and the distinguishing features required for the process design kits (PDK) and the design tools for cryogenic integrated circuits. Those challenges will thus define a roadmap for cryogenic electronics as a crucial enabling technology for future large-scale quantum computers.

FS03.4 Software for Quantum Computing

Robert Wille, TU Munich, DE

Abstract: In the classical computing realm, software is omnipresent and not only used to realize applications but is essential in the design of electronic circuits and systems themselves. For the quantum realm, similar developments are currently emerging. But these tools do not (yet) fully utilize experiences gained in the field of design automation over the last decades. This leaves huge potential for further improvement untapped. In fact, many of the design problems considered for quantum computing are of combinatorial and exponential nature ---a complexity with which design automation experts are quite familiar with. In this talk, a selection of design tasks is discussed, for which software and particularly design automation background can be utilized. The corresponding solutions are available through the Munich Quantum Toolkit (MQT) which offers open-source implementations for these tasks (available at https://www.cda.cit.tum.de/research/quantum/mqt). By this, an overview of the full spectrum of tasks is provided where dedicated software can be useful and, in fact, is required.

Date: Wednesday, 27 March 2024

Time: 16:30 - 18:00 CET

FS04 Focus Session: Panel On Resilience Of Deep Learning Applications: Where We Are And Where We Want To Go

Session chair: Krishnendu Chakrabarty, Arizona State University, US
Session chair: Alberto Bosio, Ecole Centrale de Lyon, FR
Organisers: Cristiana Bolchini, Politecnico di Milano, IT, Alberto Bosio, Ecole Centrale de Lyon, FR
Panellists: Annachiara Ruospo, Politecnico di Torino, IT, Paolo Rech, Università di Trento, IT, Maksim Jenihhin, Tallinn University of Technology, EE, Masanori Hashimoto, Kyoto University, JP, Luciano Ost, Loughborough University, GB, Muhammad Shafique, New York University Abu Dhabi, AE

Hardware for AI (HW-AI), similar to traditional computing hardware, is subject to hardware faults (HW faults) that can have several sources: variations in fabrication process parameters, fabrication process defects, latent defects, i.e., defects undetectable at time-zero post-fabrication testing that manifest themselves later in the field of application, silicon ageing, e.g., time-dependent dielectric breakdown, or even environmental stress, such as heat, humidity, vibration, and Single Event Upsets (SEUs) stemming from ionization. All these HW faults can cause operational failures, potentially leading to important consequences, especially for safety-critical systems. This panel aims at gathering the various contributors of this scientific community, to discuss the milestones reached so far and the future directions in the form of open challenges to be addressed. The panel format will be exploited to involve the audience (DATE community is very active on the topic) to make the conversation as inclusive as possible, to actually allow for a broader view on the matter.

Date: Monday, 25 March 2024
Time: 11:00 - 12:30 CET

FS05 Focus Session: Evolution Of MI Hardware: From Technologies To Algorithms And Architectures

Session chair: Krishnendu Chakrabarty, Arizona State University, US
Session co-chair: Hussam Amrouch, TU Munich (TUM), DE
Organiser: Partha Pande, Washington State University, US

Training and executing emerging machine learning (ML) workloads are computationally demanding. For this reason, the industrial trend is to design specialized chips to accelerate ML workloads to efficiently process almost any kind of data, including images, text, audio, or biosensed signals. Google's Tensor Processing Unit (TPU), for instance, accelerates deep neural network (DNN) inference and training using a systolic array, a precisely timed array containing thousands of multiply-and-accumulate (MAC) units. However, there remain many open challenges with the design of energy-efficient and reliable DNN and other ML model accelerators, including technology selection, circuit design, architecture exploration, and mapping computations, data, and communication to hardware in a scalable manner. With the rising needs of advanced algorithms for large-scale data analysis and data-driven discovery, and significant growth in emerging applications from the edge to the cloud, we need low-cost, high-performance, energy-efficient, and reliable computing systems targeted for these applications. As an example, the emergence of large language models (LLMs) that rely on deep transformer neural networks and big data processing that increasingly relies on large graph neural networks, there is a need to explore new paradigms to support ultra-high throughput and energy-efficient computation, storage, and communication in the next generation of ML accelerators. The presenters will describe the most-compelling research advances and architectural breakthroughs that will contribute to closing the gap between hype and reality in ML accelerator design.

FS05.1 Algorithm to Technology Co-Optimization for CiM-based Hyperdimensional Computing

Mahta Mayahinia[1], Simon Thomann[2], Paul Genssler[3], Christopher Münch[1], Hussam Amrouch[4] and Mehdi Tahoori[1]
[1]Karlsruhe Institute of Technology, DE; [2]Chair of AI Processor Design, TU Munich (TUM), DE; [3]University of Stuttgart, DE; [4]TU Munich (TUM), DE
Abstract: Hyperdimensional computing (HDC) has been recognized as an efficient machine learning algorithm in recent years. Robustness against noise, and simple computational operations, while being limited by the memory bandwidth, make it a perfect fit for the concept of computation in memory (CiM) with emerging nonvolatile memory (NVM) technologies. For an HDC accelerator based on NVM-CiM, there are different parameters from the algorithm all the way down to the technology that interact with

each other and affecting the overall inference accuracy as well as the energy efficiency of the accelerator. Therefore, in this paper, we propose, for the first time, a full-stack co-optimization method and use it to design an HDC accelerator based on NVM-based content addressable memory (CAM). By incorporating the device manufacturing variability and co-optimizing the algorithm and hardware design, HDC inference on our proposed NVM-based CiM accelerator can reduce the energy consumption by 3.27x, while compared to the purely software-based implementation, the inference accuracy loss is merely 0.125%.

FS05.2 Accelerating Neural Networks for Large Language Models and Graph Processing with Silicon Photonics

Salma Afifi, Febin Sunny, Mahdi Nikdast and Sudeep Pasricha, Colorado State University, US

Abstract: In the rapidly evolving landscape of artificial intelligence, large language models (LLMs) and graph processing have emerged as transformative technologies for natural language processing (NLP), computer vision, and graph-structured data applications. However, the complex structures of these models pose challenges for acceleration on conventional electronic platforms. In this paper, we describe novel hardware accelerators based on silicon photonics to accelerate transformer neural networks that are used in LLMs and graph neural networks for graph data processing. Our analysis demonstrates that both hardware accelerators achieve at least 10.2× throughput improvement and 3.8× better energy efficiency over multiple state-of-the-art electronic hardware accelerators designed for LLMs and graph processing.

FS05.3 Dataflow-Aware PIM-Enabled Manycore Architecture for Deep Learning Workloads

Harsh Sharma[1], Gaurav Narang[1], Jana Doppa[1], Umit Ogras[2] and Partha Pratim Pande[1]
[1]Washington State University, US; [2]University of Wisconsin Madison, Madison, US

Abstract: Processing-in-memory (PIM) has emerged as an enabler for the energy-efficient and high-performance acceleration of deep learning (DL) workloads. Resistive random-access memory (ReRAM) is one of the most promising technologies to implement PIM. However, as the complexity of Deep convolutional neural networks (DNNs) grows, we need to design a manycore architecture with multiple ReRAM-based processing elements (PEs) on a single chip. Existing PIM-based architectures mostly focus on computation while ignoring the role of communication. ReRAM-based tiled manycore architectures often involve many Processing Elements (PEs), which need to be interconnected via an efficient on-chip communication infrastructure. Simply allocating more resources (ReRAMs) to speed up only computation is ineffective if the communication infrastructure cannot keep up with it. In this paper, we highlight the design principles of a dataflow-aware PIM-enabled manycore platform tailor-made for various types of DL workloads. We consider the design challenges with both 2.5D interposer- and 3D integration-enabled architectures.

Date: Tuesday, 26 March 2024
Time: 16:30 - 18:00 CET

FS06 Focus Session: Resilient Cognitive Sensing And Inference In Distributed And Dynamic Environments

Session chair: Kaushik Roy, Purdue University, US
Organiser: Amit Ranjan Trivedi, University of Illinois at Chicago, US

In the rapidly evolving technological era, a seamless fusion of the physical and digital realms is more critical than ever. This special session will focus on one of the recent pivotal innovations to facilitate this integration through cognitive sensing. Rather than relying on traditional sensing mechanisms that often capture excessive and potentially redundant data—leading to the challenge of the analog data deluge—cognitive sensing offers an intelligent approach. By discerning and interpreting environmental cues, it filters out the noise, ensuring only pertinent data is processed and utilized. To further leverage the abilities of cognitive sensing in distributed and dynamic environments, the special session will also focus on the bridge from cognitive sensing to neuromorphic computing and distributed inference. Distributed inference decentralizes the computation process, allowing for data-driven decisions to be made closer to the source, such as edge devices. This decentralization not only reduces latency but also ensures more efficient data processing in real-time scenarios. Neuromorphic computing, on the other hand, seeks inspiration from the human brain. By mimicking neural structures and functions, neuromorphic systems achieve unparalleled energy efficiency and processing capabilities, especially vital for real-time dynamic environments. Both of these frameworks leverage and benefit cognitive sensing by seamlessly merging sensing and inference in a unified framework over a network of inference devices. Finally, while most data-driven models act as black boxes, lacking interpretability and theoretical guarantees on prediction quality, thus creating challenges for mission-critical applications like autonomous vehicles, the special session will also focus on

uncertainty estimation at the edge where the predictive models know when they don't know. Especially, current approaches for uncertainty-aware inference, such as Bayesian neural networks (BNNs), demand excessive computations, prohibitive under time, energy, and area constraints at the edge. To overcome this critical challenge, the special session will also focus on computationally efficient uncertainty estimation at the edge so that the downstream processing is aware of prediction risks.

FS06.1 HaLo-FL: Hardware-Aware Low-Precision Federated Learning

Yeshwanth Venkatesha, Abhiroop Bhattacharjee, Abhishek Moitra and Priyadarshini Panda, Yale University, US

Abstract: Applications of federated learning involve devices with extremely limited computational resources and often with considerable heterogeneity in terms of energy efficiency, latency tolerance, and hardware area. Although low-precision training methods have demonstrated effectiveness in accommodating the device constraints in a centralized setting, their applicability in distributed learning scenarios featuring heterogeneous client capabilities has not been well explored. In this work, we design a hardware-aware low-precision federated training framework (HaLo-FL) tailored to heterogeneous resource-constrained devices. In particular, we optimize the precision for weights, activations, and errors for each client's hardware constraint using a precision selector (named HaLo-PS). To validate our approach, we propose HaLoSim, a hardware evaluation platform that enables precision reconfigurability and evaluates hardware metrics like energy, latency, and area utilization on a crossbar-based In-memory Computing (IMC) platform.

FS06.2 Cognitive Sensing for Energy-efficient Edge Intelligence

Minah Lee, Sudarshan Sharma, Wei Chun Wang, Hemant Kumawat, Nael Rahman and Saibal Mukhopadhyay, Georgia Tech, US

Abstract: Edge platforms in autonomous systems integrate multiple sensors to interpret their environment. The high-resolution and high-bandwidth pixel arrays of these sensors improve sensing quality but also generate a vast, and arguably unnecessary, volume of real-time data. This challenge, often referred to as the analog data deluge, hinders the deployment of high-quality sensors in resource-constrained environments. This paper discusses the concept of cognitive sensing, which learns to extract low-dimensional features directly from high-dimensional analog signals, thereby reducing both digitization power and generated data volume. First, we discuss design methods for analog-to-feature extraction (AFE) using mixed-signal compute-in-memory. Next, we then present examples of cognitive sensing, incorporating signal processing or machine learning, for various sensing modalities including vision, Radar, and Infrared. Subsequently, we discuss the reliability challenges in cognitive sensing, taking into account hardware and algorithmic properties of AFE. The paper concludes with discussions on future research directions in this emerging field of cognitive sensors.

FS06.3 Unearthing the Potential of Spiking Neural Networks

Sayeed Shafayet Chowdhury, Adarsh Kosta, Deepika Sharma, Marco Apolinario and Kaushik Roy, Purdue University, US

Abstract: Spiking neural networks (SNNs) are a promising avenue for machine learning with superior energy efficiency compared to traditional artificial neural networks (ANNs). Recent advances in training and input encoding have put SNNs on par with state-of-the-art ANNs in image classification. However, such tasks do not utilize the internal dynamics of SNNs fully. Notably, a spiking neuron's membrane potential acts as an internal memory, merging incoming inputs sequentially. This recurrent dynamic enables the networks to learn temporal correlations, making SNNs suitable for sequential learning. Such problems can also be tackled using ANNs. However, to capture the temporal dependencies, either the inputs have to be lumped over time (e.g. Transformers); or explicit recurrence needs to be introduced (e.g. recurrent neural networks (RNNs), long-short-term memory (LSTM) networks), which incurs considerable complexity. To that end, we explore the capabilities of SNNs in providing lightweight solutions to four sequential tasks involving text, speech and vision. Our results demonstrate that SNNs, by leveraging their intrinsic memory, can be an efficient alternative to RNNs and LSTMs for sequence processing, especially for certain edge applications. Furthermore, SNNs can be combined with ANNs (hybrid networks) synergistically to obtain the best of both worlds in terms of accuracy and efficiency.

Navigating the Unknown: Uncertainity-Aware Autonomy of Edge Robotics with Compute-in-Memory

Nastaran Darabi[1], Priyesh Shukla[2], Dinithi Jayasuriya[1], Divake Kumar[1], Alex Stutts[1] and Amit Trivedi[1]
[1]University of Illinois at Chicago, US; [2]Samsung, IN

Abstract: This paper addresses the challenging problem of energy-efficient and uncertainty-aware pose estimation in insect-scale drones, which is crucial for tasks such as surveillance in constricted spaces and for enabling non-intrusive spatial intelligence in smart homes. Since tiny drones operate in highly

dynamic environments, where factors like lighting and human movement impact their predictive accuracy, it is crucial to deploy uncertainty-aware prediction algorithms that can account for environmental variations and express not only the prediction but also confidence in the prediction. We address both of these challenges with Compute-in-Memory (CIM) which has become a pivotal technology for deep learning acceleration at the edge. While traditional CIM techniques are promising for energy-efficient deep learning, to bring in the robustness of uncertainty-aware predictions at the edge, we introduce a suite of novel techniques: First, we discuss CIM-based acceleration of Bayesian filtering methods uniquely by leveraging the Gaussian-like switching current of CMOS inverters along with co-design of kernel functions to operate with extreme parallelism and with extreme energy efficiency. Secondly, we discuss the CIM-based acceleration of variational inference of deep learning models through probabilistic processing while unfolding iterative computations of the method with a compute reuse strategy to significantly minimize the workload. Overall, our co-design methodologies demonstrate the potential of CIM to improve the processing efficiency of uncertainty-aware algorithms by orders of magnitude, thereby enabling edge robotics to access the robustness of sophisticated prediction frameworks within their extremely stringent area/power resources.

Date: Monday, 25 March 2024
Time: 16:30 - 18:00 CET

FS07 Focus Session: Formal Verification Under Resource Constraints

Session chair: Rolf Drechsler, University of Bremen | DFKI, DE
Organiser: Lukas Sekanina, Brno University of Technology, CZ

Formal verification is almost always connected with constrained resources, e.g., the runtime of a given formal verification technique is constrained by available time or resources, or a verification technique can have some principal applicability constraints. The role of constraints thus becomes crucial and, in fact, determines whether a formal verification technique can be applied or not. The objective of this proposal is to (a) present current trends in formal verification methods working under various resource constraints, (b) highlight successful results, and (c) discuss possible future developments.

FS07.1 Polynomial Formal Verification of Sequential Circuits

Caroline Dominik[1] and Rolf Drechsler[2]
[1]Institute of Computer Science, University of Bremen/DFKI, DE; [2]University of Bremen | DFKI, DE
Abstract: Recently, the concept of Polynomial Formal Verification (PFV) has been introduced and successfully applied to several classes of functions, allowing complete verification under resource constraints. But so far, all studies were carried out for combinational circuits only. In this paper we show how the concept of PFV can be extended to sequential circuits. As a first case study we show for counters that PFV can be performed, even though they have an exponential number of states, i.e., they can be fully formally verified within polynomial upper bounds on run-time and memory requirement.

FS07.2 Automated Verifiability-Driven Design of Approximate Circuits: Exploiting Error Analysis

Zdenek Vasicek, Vojtech Mrazek and Lukas Sekanina, Brno University of Technology, CZ
Abstract: A fundamental assumption for search-based circuit approximation methods is the ability to massively and efficiently traverse the search space and evaluate candidate solutions. For complex approximate circuits (adders and multipliers), common error metrics, and error analysis approaches (SAT solving, BDD analysis), we perform a detailed analysis to understand the behavior of the error analysis methods under constrained resources, such as limited execution time. In addition, we show that when evaluating the error of a candidate approximate circuit, it is highly beneficial to reuse knowledge obtained during the evaluation of previous circuit instances to reduce the total design time. When an adaptive search strategy that drives the search towards promptly verifiable approximate circuits is employed, the method can discover circuits that exhibit better trade-offs between error and desired parameters (such as area) than the same method with unconstrained verification resources and within the same overall time budget. For 16-bit and 20-bit approximate multipliers, it was possible to achieve a 75\% reduction in area when compared with the baseline method.

FS07.3 Using Formal Verification Methods for Optimization of Circuits under External Constraints

Daniel Grosse, Lucas Klemmer and Dominik Bonora, Johannes Kepler University Linz, AT
Abstract: This paper targets the optimization of circuit netlists by eliminating redundant gates under given external constraints. Typical examples for external constraints – which can be viewed as external

don't cares – are restrictions on input operands, instruction subsets used by a processor for specific applications, or limited operation modes of an integrated IP block. Targeting external don't cares presents a challenge because the optimization problem changes from a completely specified Boolean function to a Boolean relation. We propose an optimization approach that utilizes formal verification methods. We demonstrate how to formulate Property Checking (PC) and Equivalence Checking (EC) problems to determine if a gate is redundant under given external constraints. Essentially, the validity of up to four rules must be checked per gate. We show that these checks can be solved concurrently, resulting in faster overall optimization. We have implemented our approach as the tool Formal SYNthesis (FSYN). FSYN utilizes open-source tools to scale the solving of formal instances with available hardware resources. We demonstrate that our approach can achieve substantial reductions in the number of gates for combinational circuits under given external constraints.

FS07.4 Combining Formal Verification and Testing for Debugging of Arithmetic Circuits

Jiteshri Dasari and Maciej Ciesielski, University of Massachusetts Amherst, US

Abstract: Formal verification has been successfully used to verify different types of digital circuits, including combinational and sequential logic, arithmetic circuits, and datapath designs. However, the verification techniques concentrate on confirming whether the circuit performs its intended function, while the issue of debugging, i.e., detection and correction of functional errors of the design, remains an open problem. Elaborate testing techniques have been developed that target certain types of manufacturing faults but there are no general techniques that address the debugging issue for functional bugs. This paper addresses the issue of debugging of arithmetic circuits that due to their large size and complexity are particularly hard to verify and debug. Current debugging techniques handle only simple types of bugs: gate replacement, wrong gate polarity, or a missing gate, but cannot handle more realistic faults, such as wrong wiring or using a wrong combination of logic gates. We describe a novel method that combines formal verification and testing techniques to enable efficient identification and correction of faults. The technique involves setting select signals to some predefined constants to reduce the design to easily verifiable circuit components; these components are then verified using logic equivalence checking and SAT tools. The fault can then be identified in form or a small logic area (with a few logic gates) to be replaced by a new, functionally correct logic. The proposed technique is illustrated with debugging of different types of divider circuits up to 1024 bit-wide.

Date: Tuesday, 26 March 2024
Time: 11:00 - 12:30 CET

FS08 Panel session: How to Attract, Train and Keep more Talent to Science & Semiconductor

Session chair: Catherine Le Lan, Synopsys, FR
Organisers: Catherine Le Lan, Synopsys, FR; Olivier Sentieys, Inria, FR

The microelectronics landscape is evolving, currently driven by AI and the adoption of the chiplets. With chips being an integral part of our daily lives, there is a crucial emphasis on the computing power, security, safety, and efficiency of chips. To address the future semiconductor demand and fuel a pipeline of skilled talent, this session aims to discuss strategies that unite the broader microelectronics ecosystem to collaboratively address workforce development needs.

Cultivating a Diverse Workforce to Meet EU Chips Act Ambitions

Laith Altimime, SEMI Europe, DE

Abstract: Talent remains as one of the industry's most pressing global challenge. To achieve the EU Chips Act Ambitions by achieving 20% of the global market share by 2030 we will need to more than double the current workforce in Europe and with more diverse skills. We will need to explore new strategies to Scale-Up initiatives to populate the talent pipeline. Strategies include scaled-up funding mechanisms at national and global levels by establishing global and regional Industry – Academia partnerships with focus on Diversity, Upskilling, Reskilling and Retention of the future workforce, as well as collaborative global initiatives to attract and facilitate talent mobility for a diverse international workforce.

What are the University Challenges to Train More Students?

John Goodenough, Manchester University, UK

Abstract: We often talk about a skills gap and not having enough talent for open vacancies in the industry. In this short presentation we will take a look at where the 'people' come from or could come from. What

pathways exist to develop the talent our industry needs. What sort of education do they need, how does this similar to the training that is needed to be successful in industry. When is it appropriate for example to do tools specific training vs teaching general principals. We will look at some of the constraints in academia, curriculum, assessment requirement, the availability of inspiring instructors and general pressures within the sector. I will conclude with a short call to action to the industry and government as to how they might constructively align agendas to develop the talent capability - (hint I don't think the way we are doing it now is working all that well) - that is needed in the future and some ideas on how we might solve the 1-3 year challenge we face more immediately.

Meeting Industry Needs for Tomorrow's Chip Design Work Force

Yervant Zorian, Synopsys, US

Abstract: As chip design requirements continue to change, tomorrow's work force needs to perform new types of activities and require corresponding preparation. A well-defined collaboration between academia and chip design industry is necessary to prepare tomorrow workforce during its education stage, in order to utilize advanced ML-based EDA tools, embedded firmware, high performance interface IP subsystems, chiplets for 2.5/3D multi-die designs. This presentation will cover a particular educational model developed by Synopsys Armenia Educational Department to prepare for tomorrow's work force and implemented in partnership with several academic institutions.

How to Ensure Existing Engineers are Trained on Tomorrow's Challenges?

Peter Groos, Cadence Design Systems, DE

Abstract: The increasing demand for engineers in the semiconductor industry in the next 5 to 10 years requires strategies and programs including national or regional funding to reduce the workforce and educational gap. The effect of these programs is rather mid to long term and yet to be proven. Under the assumption that the shortage will prevail measures need to be taken to continuously develop and maintain the knowledge and skill set of today's engineering teams to create future products and solutions in the most efficient ways. Work force development programs help to develop new skills through re-skilling or up-skilling. Furthermore, prediction of market trends and agility to adopt to new demands are key in having the right skill sets when they are needed. For a successful implementation these programs need to be centered around the individual embedded in an inclusive team culture.

Date: Wednesday, 27 March 2024
Time: 8:30 - 10:00 CET

FS09 Focus session: AI for EDA, and EDA for AI

Session chair: Anuj Pathania, University of Amsterdam, NL
Session co-chair: Todor Stefanov, Leiden University, NL
Organisers: Catherine Le Lan, Synopsys, FR; Olivier Sentieys, Inria, FR

AI – The Next Revolution in Chip Design Automation

Tobias Bjerregaard, Synopsys, DK

Abstract: AI is making great strides and in particularly the generative AI technologies are set to transform entire industries. AI-based chip design flows are not only yielding better results, but also improving designer productivity by automating many of the tasks traditionally done by human experts. In this talk I will outline key uses of AI in the chip design process. I will look across the entire EDA stack at where AI-based approaches have made the highest impact. I will also look at how generative AI technologies can help capture human knowhow and as such be particularly powerful in mitigating the talent gap that the chip design industry is facing.

Automation in Deep Learning and Hardware Integration

Dolly Sapra, University Van Amsterdam, NL

Abstract: This talk focuses on how EDA tools are changing the way deep learning models are integrated with hardware, especially in edge devices. Tools to automatically identify the most suitable deep learning models for specific hardware configurations are discussed. These methods are crucial for a large number of edge devices, where limitations in power and processing capacity are often encountered. The talk further elaborates on the methods to achieve efficient system-resource management, ensuring that neural network layers are meticulously mapped to the most appropriate hardware components. This approach not only enhances the computational efficiency of edge devices but also contributes significantly to their energy conservation. The aim of this talk is to highlight the developments and opportunities of automating deep learning inference, at a time when AI is increasingly present in every aspect of our lives and becoming integral to the devices we use every day.

Designing the future chips: A-DECA synergizes AI and Optimization techniques for Automatic Architecture Exploration

Lilia Zaourar, CEA LIST, FR

Abstract: Nowadays, chip designers face various challenges due to the short time to market, increased system complexity, computing heterogeneity, and various SW/HW constraints. Usually, traditional solutions are based on prior engineering experience from computer architects. However, finding a suitable architecture that can accommodate a good balance between various Key Performance Indicators is a notorious problem because of two issues: 1) design space is extremely large, and its size grows exponentially when adding new components, and 2) computing cost is large, in particular for metrics evaluation. A-DECA (Automated Design space Exploration for Computing Architectures) framework leverages various Combinatorial Optimization techniques and Machine Learning strategies to achieve an efficient trade-off on the usual PPA (Performance, Power, Area) but also includes other ones such as security and sustainability. A concrete use case focusing on the design of the next generation of exascale processors for HPC will be presented.

Date: Monday, 25 March 2024
Time: 14:00 - 15:30 CET

FS10 Focus session: Chip Design Enablement: How to lower barriers to hardware design with high level languages, generative AI, and Cloud

Session chair: Olivier Sentieys, Inria, FR
Organisers: Catherine Le Lan, Synopsys, FR; Olivier Sentieys, Inria, FR

Writing software to elaborate hardware (SpinalHDL)

Charles Papon, Independent, CH

Abstract: This talk will provide an overview about how software approaches can be used to capture hardware specifications and generate their corresponding Verilog/VHDL "netlist ». The main motivation for such approach being to go beyond what the System-Verilog and VHDL tooling support in terms of hardware elaboration, increasing developer productivity, being able to build hardware generation abstractions while keeping full control over the generated hardware. Another motivation is also to be able to use an extendable tool, meaning, not having to restrict yourself to baked-in features, but instead being able to extend the scope of the tool, avoiding having to switch between different languages, and so avoiding a flow fracture or mismatch. This talk will be based around the recents developments made on VexiiRiscv (a RISC-V multi-issue processor softcore), including its hardware pipelining API and scheduler generation which are based on Scala (a general purpose programming language) and SpinalHDL (a Scala library providing a hardware description API).

VeriHDL: Enforcing Correctness in LLM-Generated HDL

Valerio Tenace and Pierre-Emmanuel Gaillardon, PrimisAI, US

Abstract: Over the past few months, the rapid proliferation of Large Language Models (LLMs) for Hardware Description Language (HDL) generation has attracted considerable attention. These technologies, by automating complex design tasks, aim to streamline workflows and hasten the innovation process. However, the intrinsic probabilistic nature of LLMs introduces a degree of uncertainty, often manifesting as errors or hallucinations in the generated HDL code—a matter of great concern in the realm of hardware design where accuracy is non-negotiable. To tackle this issue, we present VeriHDL, a novel LLM-based framework tailored to bolster the accuracy and dependability of HDL code produced by generative artificial intelligence. Central to VeriHDL is a harmonious blend of sophisticated and interconnected LLMs that enable: (1) a systematic HDL generation process that leverages a dedicated knowledge base of pre-defined and verified IPs as an initial safeguard against most common mistakes, (2) an automated and iterative testbench generation mechanism, to enforce functional correctness, and (3) a seamless interface with Electronic Design Automation tools, as to enable an automatic verification process with no-human-in-the-loop. This innovative and original approach, currently in its early beta stage within PrimisAI's RapidGPT platform, is not only meant to improve the accuracy of generated code, but also to significantly reduce the time and resources required for verification. As a result, VeriHDL represents a substantial paradigm shift in hardware design, facilitating a more efficient, reliable, and streamlined development process. In this presentation, we will delve into the foundational principles of VeriHDL, starting with an in-depth analysis of its architecture. We will then explore the dynamic interplay among its components, illustrating how they collectively contribute to the framework's effectiveness. The session will culminate in a demonstration, showcasing VeriHDL's practical application and its impact on streamlining the hardware design process.

CUMULUS: A Cloud-Based EDA Platform for Teaching and Research

Phillip Christie, Trinity College Dublin, IE

Abstract: In this presentation, I will relate our early experiences in the development and deployment of a cloud-based Electronic Design Automation (EDA) platform in Microsoft Azure, to be used as the basis of a set of laboratories associated with a Masters' degree level module in microelectronics at Trinity College Dublin. The intent of the CUMULUS platform is not to implement a commercial design flow but rather to permit students to see how choices made at one stage affect performance at later stages. The flow from device model, library characterization, synthesis, place and route, to timing analysis creates a sequence of data files in standardized formats which, while being mostly text-based, are not designed for human assessment. A key design concept of the CUMULUS platform has therefore been to use a suite of specially created MATLAB toolboxes to visualise and assess these data (in liberty, LEF, DEF, timing reports, GDSII formats) generated at each stage. This presentation will end by providing an overview of costs for the lab, show examples of the graphical representation of data files and make recommendations for future improvements to the CUMULUS platform.

DATE 2024 PhD Forum

Date: Monday, 25 March 2024
Time: 18:30 - 20:00 CET

The PhD Forum is a poster session hosted by EDAA, ACM-SIGDA, and IEEE CEDA for PhD students who have completed their Ph.D. thesis within the last 12 months or are close to completing their thesis work. It represents an excellent opportunity for them to get feedback on their research and for the industry to get a glance of the state-of-the-art in system design and design automation.

Admitted Presentations

PROCESSING-IN-MEMORY ARCHITECTURES FOR GRAPH PROCESSING
Yu Huang, Huazhong University of Science and Technology, CN

REVOLUTIONIZING CRYOGENIC COMPUTING THROUGH FERROELECTRIC-SUPERCONDUCTOR INTERPLAY
Shamiul Alam, University of Tennessee Knoxville, USA

HARDWARE DESIGNS FOR SECURE MICROARCHITECTURES
Jan Thoma and Tim Güneysu, Ruhr-University Bochum, DE

DYNAMO: A FRAMEWORK TO OPTIMIZE, VERIFY AND RECONFIGURE FLEXIBLE MANUFACTURING SYSTEMS
Sebastiano Gaiardelli and Franco Fummi, University of Verona, IT

DESIGN AUTOMATION TOOLS AND SOFTWARE FOR QUANTUM COMPUTING
Lukas Burgholzer, Technical University of Munich, DE

HW-SW CO-EXPLORATION AND OPTIMIZATION FOR NEXT-GENERATION LEARNING MACHINES
Chunyun Chen and Mohamed M. Sabry Aly, Nanyang Technological University, SG

DYNAMIC MEMORY MANAGEMENT TECHNIQUES FOR OPTIMIZATION OVER HETEROGENEOUS DRAM/NVM SYSTEMS
Manolis Katsaragakis[1], Francky Catthoor[2] and Dimitrios Soudris[1], [1]National Technical University of Athens, GR; [2]IMEC, BE

INTEGRATING BIOLOGICAL AND ARTIFICIAL NEURAL NETWORKS PROCESSING ON FPGAS
Gianluca Leone and Paolo Meloni, Università degli Studi di Cagliari, IT

ENHANCING SECURITY FEATURES OF NETWORK-ON-CHIP
Syam Sankar and John Jose, Indian Institute of Technology Guwahati, IN

REINFORCEMENT LEARNING FRAMEWORKS FOR PROTECTING INTEGRATED CIRCUITS
Vasudev Gohil, Texas A&M University; USA

EFFICIENT DEPLOYMENT OF EARLY-EXIT DNN ARCHITECTURES ON FPGA PLATFORMS
Anastasios Dimitriou, Geoff Merrett and Jonathon Hare, University of Southampton, UK

FORMALLY PROVED MEMORY CONTROLLERS
Felipe Lisboa Malaquias, Télécom Paris, FR

EFFICIENT HARDWARE ACCELERATOR FOR CONVOLUTIONAL NEURAL NETWORK BASED INFERENCE ENGINES
Deepika S and Arunachalam V, VIT, IN

OPTIMIZING NEURAL NETWORKS FOR EMBEDDED EDGE-PROCESSING PLATFORMS
Paola Busia and Paolo Meloni, DIEE, Università degli Studi di Cagliari, IT

SECURITY VALIDATION OF SYSTEMS IMPLEMENTATIONS
Aruna Jayasena, University of Florida, USA

ARCHITECTING FAST AND ENERGY-EFFICIENT HARDWARE ACCELERATORS FOR EMERGING ML WORKLOADS USING HARDWARE-SOFTWARE CO-DESIGN
Tom Glint, Indian Institute of Technology Gandhinagar, IN

OPTIMIZED FLOATING-POINT ARITHMETIC UNIT FOR EFFICIENT OPERATIONS IN DNN ACCELERATORS
Jing Gong and Sri Parameswaran, The University of New South Wales, AU

INVESTIGATION OF SENSITIVITY OF DIFFERENT LOGIC AND MEMORY CELLS TO LASER FAULT INJECTIONS
Dmytro Petryk, IHP – Leibniz-Institut für innovative Mikroelektronik, DE

HORIZONTAL ADDRESS-BIT SCA ATTACKS AND COUNTERMEASURES
Ievgen Kabin, IHP – Leibniz-Institut für innovative Mikroelektronik, DE

POWER-SUPPLY NOISE MONITORING TO EVALUATE EMBEDDED VRMS AND SI-BACKSIDE BURRIED DECAPS
Kazuki Monta and Makoto Nagata, Kobe University, JP

MODELING ENERGY AND PERFORMANCE IN ENERGY HARVESTING IOT SYSTEMS
Fatemeh Ghasemi and Magnus Jahre, Norwegian University of Science and Technology, NO

THIN-FILM COMPUTE-IN-MEMORY CIRCUITS AND SYSTEMS FOR LARGE-AREA SENSING APPLICATIONS
Jialong Liu, Huazhong Yang and Xueqing Li, Tsinghua University, CN

OPERATIONAL DATA ANALYTICS IN HPC: TOWARDS ANOMALY PREDICTION
Martin Molan and Andrea Bartolini, University of Bologna, IT

DYNAMIC DNNS AND RUNTIME MANAGEMENT FOR EFFICIENT INFERENCE ON MOBILE/EMBEDDED DEVICES
Lei Xun, Jonathon Hare and Geoff Merrett, University of Southampton, UK

DESIGN METHODOLOGIES AND ARCHITECTURES FOR APPLICATION-SPECIFIC COARSE-GRAIN RECONFIGURABLE ACCELERATORS
Francesco Ratto, Università degli Studi di Cagliari, IT

EFFICIENT SYNTHESIS METHODS FOR HIGH-QUALITY APPROXIMATE COMPUTING CIRCUITS AND ARCHITECTURES
Chang Meng, EPFL, CH

AUTOMATIC HARDWARE-AWARE DESIGN AND OPTIMIZATION OF DEEP LEARNING MODELS
Matteo Risso, Massimo Poncino and Daniele Jahier Pagliari, Politecnico di Torino, IT

LEVERAGE WIFI CHANNEL STATE INFORMATION AND WEARABLE SENSORS FOR HUMAN MONITORING
Cristian Turetta and Graziano Pravadelli, University of Verona, IT

VERSATILE HARDWARE ANALYSIS TECHNIQUES - FROM WAVEFORM-BASED ANALYSIS TO FORMAL VERIFICATION
Lucas Klemmer and Daniel Grosse, Johannes Kepler University Linz, AT

EFFICIENT SECURITY FOR EMERGING COMPUTING PLATFORMS: SIDE-CHANNEL ATTACKS AND DEFENSES
Mahya Morid Ahmadi[1] and Muhammad Shafique[2], [1]Technische Universität Wien, AT; [2]New York University Abu Dhabi, UAE

ASSESSING THE RELIABILITY OF THE SKYWATER 130NM PDK FOR FUTURE SPACE PROCESSORS
Ivan Rodriguez Ferrandez and Leonidas Kosmidis, Barcelona Supercomputing Center and Universitat Politècnica de Catalunya, ES

A SELF-ADAPTIVE RESILIENT METHOD FOR IMPLEMENTING AND MANAGING THE HIGH-RELIABILITY PROCESSING SYSTEM
Junchao Chen and Milos Krstic, IHP GmbH - Innovations for High Performance Microelectronics, DE

SYNERGISTIC SOFTWARE-HARDWARE APPROXIMATION AND CO-DESIGN FOR MACHINE LEARNING CLASSIFICATION IN PRINTED ELECTRONICS
Giorgos Armeniakos[1], Dimitrios Soudris[1] and Joerg Henkel[2], [1]National Technichal University of Athens, GR; [2]Karlsruhe Institute of Technology, DE

SECURING NANO-CIRCUITS AGAINST OPTICAL PROBING ATTACK
Sajjad Parvin and Rolf Drechsler, University of Bremen, DE

FAULT-BASED ANALYSIS COVERING THE ANALOG SIDE OF A SMART OR CYBER-PHYSICAL SYSTEM
Nicola Dall'Ora, University of Verona, IT

EXPONENT SHARING FOR MODEL COMPRESSION
Prachi Kashikar, Indian Institute of Technology Goa, IN

CONTRIBUTIONS TO IMPROVE THE ENERGY EFFICIENCY OF FPGA-BASED APPLICATIONS
Christoph Niemann and Dirk Timmermann, University of Rostock, DE

SCALABLE AND EFFICIENT METHODS FOR UNCERTAINTY ESTIMATION AND REDUCTION IN DEEP LEARNING
Soyed Tuhin Ahmed and Mehdi Tahoori, Karlsruhe Institute of Technology, DE

DESIGNING AND PROGRAMMING MASSIVELY PARALLEL SYSTEMS
Samuel Riedel[1] and Luca Benini[1,2], [1]ETH Zurich, CH; [2]Università di Bologna, IT

ACCELERATION OF DNA ALIGNMENT TOOLS USING HARDWARE-SOFTWARE CO-DESIGN
Kisaru Liyanage, Hasindu Gamaarachchi and Sri Parameswaran, The University of New South Wales, AU

AN ML-BASED SYSTEM-LEVEL FRAMEWORK FOR BACK-ANNOTATING LOW-LEVEL EFFECTS
Katayoon Basharkhah and Zain Navabi, University of Tehran, IR

Status: 21 February 2024

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DATE 2024 Opening Keynotes

Date: Monday, 25 March 2024
Time: 09:00 - 09:45 CET

Opening Keynote 1: Chiplet Standards: A New Route to Arm-Based Custom Silicon

Robert Dimond, ARM, United Kingdom

Abstract : A key challenge our partners are consistently looking to solve is: How can we continue to push performance boundaries, with maximum efficiency, while managing costs associated with manufacturing and yield? Today, as the ever more complex AI-accelerated computing landscape evolves, a key solution emerging is chiplets.

Chiplets are designed to be combined to create larger and more complex systems that can be packaged and sold as a single solution, made of a number of smaller dice instead of one single larger monolithic die. This creates interesting new design possibilities, with one of the most exciting being a potential route to custom silicon for manufacturers who historically chose off-the-shelf solutions.

This talk will describe two complementary approaches to realising this chiplet opportunity:

· Decomposing an existing system across multiple chiplets, in the same way a monolithic chip is composed of IP blocks.

· Aggregating well-defined peripherals across a motherboard into a single package.

Both of these approaches require collaboration in standards to align on the many non-differentiating choices in chiplet partitioning. This talk will describe the standards framework that Arm is building with our partners, and the broader industry. Including, own specifications such as the Arm Chiplet System Architecture (Arm CSA), AMBA chip-to-chip and the role of industry standards such as UCIe.

Date: Monday, 25 March 2024
Time: 09:45 - 10:30 CET

Opening Keynote 2: Enlighten your Designs With Photonic Integrated Circuits

Luc Augustin, SMART Photonics, Netherlands

Abstract: The field of integrated photonics holds great promise for overcoming societal challenges in data and telecom, autonomous driving and healthcare in terms of cost, performance, and scalability. Similar to the semiconductor industry, the ever-increasing demands of various applications are driving the necessity for platform integration in photonics as well, enabling seamless integration of diverse functionalities into compact and efficient photonic devices. This high level of integration reduces footprint and drives down system level costs. In this trend towards high levels of integration , Indium Phosphide (InP) is the material of choice for long-distance communication lasers, owing to its proven track record over several decades. Leveraging standardized fabrication processes, the cost and performance targets can be addressed. The key advantages of InP-based integration lie in its ability to fully integrate lasers, amplifiers, modulators, and passives, providing a flexible and reliable platform for building complex Photonic Integrated Circuits (PICs). This paper will address the photonic integration platforms, the applicability to current and future markets requiring the need for further heterogenous integration with other technologies, and the change to a foundry business model, much like its electronics counterpart.

DATE 2024 Lunchtime Keynotes

Date: Monday, 25 March 2024
Time: 13:15 - 14:00 CET

IEEE CEDA Distinguished Lecturer Lunchtime Keynote: AI Models for Edge Computing: Hardware-Aware Optimizations for Efficiency

Hai (Helen) Li, Duke University, United States

Abstract: As artificial intelligence (AI) transforms various industries, state-of-the-art models have exploded in size and capability. The growth in AI model complexity is rapidly outstripping hardware evolution, making the deployment of these models on edge devices remain challenging. To enable advanced AI locally, models must be optimized for fitting into the hardware constraints. In this presentation, we will first discuss how computing hardware designs impact the effectiveness of commonly used AI model optimizations for efficiency, including techniques like quantization and pruning. Additionally, we will present several methods, such as hardware-aware quantization and structured pruning, to demonstrate the significance of software/hardware co-design. We will also demonstrate how these methods can be understood via a straightforward theoretical framework, facilitating their seamless integration in practical applications and their straightforward extension to distributed edge computing. At the conclusion of our presentation, we will share our insights and vision for achieving efficient and robust AI at the edge.

Date: Tuesday, 26 March 2024
Time: 11:00 - 12:30 CET

ASD Embedded Keyote: Certainty or Intelligence: Pick One!

Edward Lee, University of California, Berkeley, United States

Abstract: Mathematical models can yield certainty, as can probabilistic models where the probabilities degenerate. The field of formal methods emphasizes developing such certainty about engineering designs. In safety critical systems, such certainty is highly valued and, in some cases, even required by regulatory bodies. But achieving reasonable performance for sufficiently complex environments appears to require the use of AI technologies, which resist such certainty. This extended abstract suggests that certainty and intelligence may be fundamentally incompatible.

Date: Tuesday, 26 March 2024
Time: 13:15 - 14:00 CET

Special Day Lunchtime Keynote: Data Center Demand Response for Sustainable Computing: Myth or Opportunity?

Ayse Coskun, Boston University, United States

Abstract: In our computing-driven era, the escalating power consumption of modern data centers, currently constituting approximately 3% of global energy use, is a burgeoning concern. With the anticipated surge in usage accompanying widespread adoption of AI technologies, addressing this issue becomes imperative. This keynote discusses a potential solution: integrating data centers into grid programs such as "demand response". This strategy not only augments power usage without necessitating new fossil-fuel infrastructure, but also facilitates more ambitious renewable deployment. However, the unique scale, operational constraints, and future projections of data centers present distinct and urgent challenges for implementing demand response. On the other hand, data centers, in contrast to other electricity consumers, boast greater flexibility in power control and offer the potential for collaborative optimization. This intersection of challenges and capabilities opens avenues for designing intelligent solutions that dynamically adjust data center power usage in response to grid requirements while meeting performance demands.

This keynote delves into the opportunities as well as the myths inherent in this perspective on improving data center sustainability. While obstacles such as creating requisite software infrastructure, establishing institutional trust, and addressing privacy concerns are prominent, the landscape is evolving. Noteworthy achievements have emerged in the development of intelligent solutions that can be swiftly implemented in data centers to accelerate demand response. These multifaceted solutions encompass dynamic power capping, load scheduling, load forecasting, market bidding, and collaborative optimization. This keynote offers insights into the exciting journey towards making sustainable computing a reality.

Date: Wednesday, 27 March 2024
Time: 13:15 - 14:00 CET

Special Day Lunchtime Keynote: Responsible Artificial Intelligence Systems: From Trustworthiness to Governance

Francisco Herrera, University of Granada, Spain

Abstract: In this plenary talk a present the general framework for designing Responsible Artificial Intelligence Systems, AI systems ensuring auditability and accountability during its design, development and use, according to specifications and the applicable regulation of the domain of practice in which the AI system is to be used. We will discuss two fundamental aspects in this kind of AI systems respecting current regulations, such as trustworthiness and governance, and the path between them.

About DATE

DATE is a leading international event providing unique networking opportunities, bringing together designers and design automation users, researchers and vendors, as well as specialists in hardware and software design, test and manufacturing of electronic circuits and systems.

The DATE 2024 conference, which is in its 27th edition, will be held at the Palacio De Congresos in Valencia (Valencia Conference Centre - VCC), Spain, from 25 to 27 March 2024, and will be chaired by Andy D. Pimentel, University of Amsterdam, NL.

DATE 2024 consolidates the renewed format that was introduced in 2023. This means that DATE 2024 again uses an intensive three-day format, focussing on interaction as well as further strengthening the community. The vast majority of regular papers will be presented in technical sessions using short flash-presentations, where the emphasis is on poster-supported live interactions (in addition to the common full-length presentation videos available before, during and after the conference). By this, we make sure that the community can actually do what conferences are for: meeting, discussing and exchanging.

Besides a record number of technical paper presentations, this year's DATE programme includes a large variety of other interesting events: Focus sessions on hot topics, Late Breaking Results sessions on breakthrough approaches and new research directions, Unplugged sessions with discussions around the "Digital Twinning" theme, embedded workshops as well as embedded tutorials, multi-partner project sessions, a new DivEDA session to increase diversity in engineering and EDA in particular, and the Young People Programme to support PhD students with their career development. Moreover, the programme also features the by now traditional Special Initiative on Autonomous Systems Design as well as two Special Days with, respectively, "Sustainable Computing" and "Responsible and Robust AI" as themes.

Valencia, situated along Spain's Mediterranean coast, is the third largest city in Spain. The city wears its history proudly while embracing the modern era. Its roots reach back to ancient Roman times, featuring historic landmarks such as the Valencia Cathedral and the imposing Torres de Serranos. But Valencia also is a city with an eye on the future. The City of Arts and Sciences, a futuristic complex, stands as a testament to its forward-thinking attitude, housing museums, an opera house, and an aquarium within its sleek modern architecture.

Beyond its historical and architectural landmarks, Valencia thrums with life and culture. The bustling Mercado Central where vendors are selling everything from fresh produce to local specialties, while the Plaza de la Virgen serves as a hub for street performers and cultural events. On top of that, Valencia's culinary scene is a feast for the senses, with its renowned paella and seafood dishes that attract food lovers from far and wide. In 2024, Valencia has also been elected as the European Green Capital, which of course perfectly aligns with DATE's Special Day on Sustainable Computing.

The Palacio de Congresos is a multi-functional building in the city of Valencia, designed for the realization of all kinds of events and conventions, especially large congresses and conferences. The building is a hallmark of architectural prowess, designed by the famous architect Norman Foster. In 2018 and 2010, the Palacio de Congresos in Valencia was designated as the World's Best Convention Centre by the International Association of Congress Palaces (AIPC), which brings together the 160 main venues in the world.

Join us in celebrating another exciting edition of the DATE conference – the top scientific event in Design, Automation, and Test of microelectronics and embedded systems for the academic and industrial research communities worldwide!

Updated information about the conference is always available online at: https://www.date-conference.com/

Design, Automation and Test in Europe Conference

The European Event for Electronic System Design & Test

Call for Papers

Scope of the Event

The 28th DATE conference is the main European event bringing together designers and design automation users, researchers and vendors as well as specialists in hardware and software design, test and manufacturing of electronic circuits and systems. DATE puts strong emphasis on both technology and systems, covering ICs/SoCs, emerging technologies, embedded systems and embedded software.

Structure of the Event

The multi-day event consists of a conference with keynote talks, regular papers, panels, hot-topic sessions, tutorials, workshops, special focus days and a track for executives. The organisation of user group meetings, fringe meetings, a Young People Programme, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design automation, design and test communities. Special space will also be allocated for multi-partner innovative research projects to show their results. More details will be available on the DATE website: http://www.date-conference.com.

Areas of Interest

Within the scope of the conference, the main areas of interest are: design automation, design tools and hardware architectures for electronic and embedded systems; test and dependability at system, chip, circuit and device level for analogue and digital electronics; modelling, analysis, design and deployment of embedded software and cyber-physical systems; application design and industrial design experiences. Topics of interest include, but are not restricted to:

- System Specification and Modelling
- System-level Design Methodologies and High-Level Synthesis
- System Simulation and Validation
- Design and Test for Analog and Mixed-Signal Circuits and Systems, and MEMS
- Design and Test of Hardware Security Primitives
- Design and Test of Secure Systems
- Formal Methods and Verification
- Network-on-Chip and on-chip Communication
- Architectural and Microarchitectural Design
- Low-power, Energy-efficient and Thermal-aware Design
- Approximate Computing
- Reconfigurable Systems
- Logical and Physical Analysis and Design
- Emerging Design Technologies for Future Computing
- Emerging Design Technologies for Future Memories
- Power-efficient and Sustainable Computing
- Smart Cities, Internet of Everything, Industry 4.0
- Automotive Systems and Smart Energy Systems
- Augmented Living and Personalized Healthcare
- Secure Systems, Circuits and Architectures
- Self-adaptive and Context-aware Systems
- Applications of Emerging Technologies
- Industrial Experiences
- Modelling and Mitigation of Defects, Faults, Variability and Reliability
- Test Generation, Test Architectures, Design for Test, and Diagnosis
- Dependability and System-Level Test
- Embedded Software Architectures, Compilers and Tool Chains
- Real-time, Dependable and Privacy-Enhanced Systems
- Machine Learning Solutions for Embedded and Cyber-Physical Systems
- Design Methodologies for Machine Learning Architectures
- Design Modelling and Verification for Embedded and Cyber-Physical Systems

Submission of Papers

All papers must be registered by Sunday, 15 September 2024 AoE (title, abstract and co-authors), the final submission of the paper to be submitted by Sunday, 22 September 2024 AoE (firm deadline) via: http://www.date-conference.com

Chairs

General Chair:
Aida Todri-Sanial
Eindhoven University of Technology, NL
Email: a.todri.sanial@tue.nl

Programme Chair:
Theocharis Theocharides, University of Cyprus, CY
Email: theocharides.theocharis@ucy.ac.cy

Conference Organisation

c/o K.I.T. Group GmbH Dresden
Bautzner Str. 117–119, 01099 Dresden, DE
Phone: +49 351 65573-137
E-mail: date@kitdresden.de